

KDJ11-A

KDJ11 CPU DIAG
CZKDJBO

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AH-T705B-MC
FICHE 01 OF 02

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The main body of the document consists of a grid of 15 columns and 15 rows of small data tables. Each table contains several columns of text, likely representing diagnostic data for the KDJ11 CPU. The text is too small to read clearly, but the layout is consistent across the grid. The tables appear to be organized into sections, with some larger tables at the top and smaller ones below. The overall appearance is that of a technical manual or diagnostic tool output.

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IDENTIFICATION

PRODUCT CODE: AC-T704B-MC
PRODUCT NAME: CZKDJ80 KDJ11 CPU DIAGNOSTIC
PRODUCT DATE: 15-MAR-84
MAINTAINER: DIAGNOSTIC ENGINEERING
AUTHORS: HENRY ENMAN, JIM PITTMAN, BARRY IRRGANG

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HISTORY

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OCT-83 REV. A
FEB-84 REV. B

FIRST RELEASE

CORRECTIONS MADE TO:

1. CORRECT VECTOR AREA MAINTENANCE PROBLEM
2. SET APT SWR TO 2000 SO THAT DEFAULT IS TO NOT TEST BEVENT WHEN IN APT ENVIRONMENT.
3. PREVENT \$TESTN FROM GETTING OUT OF SYNC WHEN SKIPPING DESELECTED TESTS.
4. PREVENT EXECUTION OF RESET INSTRUCTION TEST WHEN IN APT ENVIRONMENT.
5. CHANGE MARK INSTRUCTION TEST.
6. TURN CACHE MEMORY SYSTEM OFF DURING NON-CACHE TESTS.
7. ENSURE THAT CPU ERROR REGISTER IS CLEARED AFTER COMPLETION OF TEST THAT MIGHT CAUSE IT TO BE SET.
8. SAVE PC AND CONTENTS OF R6 ON UNEXPECTED INTERRUPTS

ADDITIONAL TESTS TO IMPROVE TEST COVERAGE INCLUDE:

1. RED ZONE TRAP TEST
2. I/O TIME OUT TRAP TEST
3. ODD ADDRESS TRAP TEST
4. PRE-FETCH BUFFER INVALIDATION TEST
5. TEST FOR SLOW C BIT ON ROR, ROL AND SXT INSTRUCTIONS
6. WAIT INSTRUCTION TEST WHEN BEVENT TEST IS SELECTED

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1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THIS IS AN APT COMPATIBLE VERSION OF THE KDJ11 CPU DIAGNOSTIC.
IT FOCUSES ON TESTING THE KDJ11 BASIC INSTRUCTION SET INCLUDING
EIS, TRAPS AND THE ALTERNATE REGISTER SET.

1.2 SYSTEM REQUIREMENTS

KDJ11-A PROCESSOR MODULE
ENSURE THAT HALT TRAP OPTION IS DISABLED (JUMPER W9 INSTALLED)
32KW MEMORY
Q-22 BACKPLANE (18 BIT QBUS MAY BE USED WITH REDUCED TEST COVERAGE)
SERIAL LINE UNIT AND CONSOLE TERMINAL (CONSOLE TERMINAL NOT REQUIRED FOR APT)

1.3 RELATED DOCUMENTS AND STANDARDS

KDJ11-A MODULE SPECIFICATION REV 2.2
PDP11 MAINDEC SYSMAC PACKAGE
J11 CONTROL CHIP SPECIFICATION 21-17679-00
J11 DATA CHIP SPECIFICATION 21-17677-00

1.4 DIAGNOSTIC HIERARCY PREREQUISITES

NONE

1.5 ASSUMPTIONS

IT IS ASSUMED THAT THE DIAGNOSTIC OPERATOR IS FAMILIAR WITH
THE XXDP+ OPERATING SYSTEM AND THE J11 MICRO-ODT.

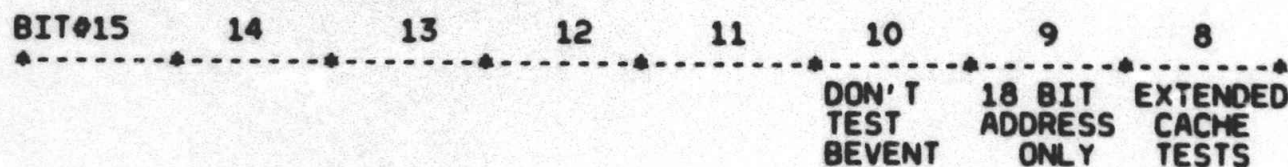
2.0 OPERATING INSTRUCTIONS

2.1 LOADING AND STARTING PROCEEDURE

LOAD PROGRAM INTO MEMORY USING STANDARD XXDP+ PROCEEDURES.
THE PROGRAM IS STARTED BY LOADING ADDRESS 200 AND USING
THE J11 MICRO-ODT G COMMAND TO START. THE PROGRAM
IDENTIFICATION MESSAGE WILL BE TYPED AFTER THE FIRST PASS
OF THE COMPLETE PROGRAM.

2.2 PROGRAM OPTIONS

THE FOLLOWING ASSIGNMENTS HAVE BEEN MADE FOR THE KDJ11-A
DIAGNOSTIC SWITCH REGISTER BITS:



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DEFAULT SETTINGS ARE TO TEST BEVENT, THE OTHER BITS HAVE NO EFFECT ON THE OPERATION OF THE CPU TEST.

TO CHANGE THE SWITCH REGISTER; HALT THE PROGRAM, LOAD THE SOFTWARE SWITCH REGISTER (ADDRESS 176) WITH THE DESIRED OPTIONS AND RESTART THE PROGRAM USING THE J11 MICRO ODT P COMMAND.

2.2 OPERATION UNDER APT

OPERATION IN THE APT ENVIRONMENT REQUIRES SOME SPECIAL CONSIDERATIONS DUE TO THE ASYNCHRONOUS HALTS OF THE DIAGNOSTIC BY THE APT MONITOR. IF THE EFFECTS OF THESE HALTS ARE NOT ANTICIPATED, FALSE ERRORS MAY BE REPORTED. THEREFORE, WHEN OPERATING IN THE APT ENVIRONMENT THE FOLLOWING DIFFERENCES IN THE EXECUTION OF THE PROGRAM SHOULD BE NOTED:

1. THE RESET INSTRUCTION TEST IS NOT EXECUTED
2. BIT 10 IN THE SOFTWARE SWITCH REGISTER IS SET SO THAT BEVENT IS NOT TESTED UNDER APT.
3. THE SERIAL LINE UNIT INTERRUPT TEST IS EXECUTED ONLY ON THE FIRST PASS OF THE PROGRAM.
4. RED ZONE TRAP TEST CHECKS FOR APT ENVIRONMENT BEFORE CALLING ERROR ROUTINE. IF IN APT MODE AND AN ERROR OCCURS, IT WILL RETRY TEST ONE MORE TIME. IF IT PASSES ON SECOND ATTEMPT, THEN FIRST ERROR WILL BE CONSIDERED TO BE APT INDUCED.

3.0 ERROR INFORMATION

ALL ERRORS WILL HALT AFTER REPORTING TO APT. ERRORS RELATING TO BOARD TESTS WILL PRINT THE FOLLOWING ERROR MESSAGE:

ERROR WHILE TESTING BOARD FUNCTIONS
ERROR # = (UNIQUE ERROR NUMBER)
ERROR PC = (PC AT TIME OF ERROR)

ERRORS RELATED TO CPU TESTS WILL PRINT THE FOLLOWING MESSAGE.

ERROR DURING CPU TESTS
ERROR # = (UNIQUE ERROR NUMBER)
ERROR PC = (PC AT TIME OF ERROR)

4.0 PROGRESS REPORT

AT THE END OF EACH PASS THE DIAGNOSTIC NAME AND PASS COUNT ARE PRINTED.

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213000001
160000.TITLE PROGRAM HEADER AND TABLES
.SBTTL PROGRAM HEADER.MCALL NEWTST,ERRDEF,,EQUAT,.KT11,,\$40CAT,,\$EOP,,\$APTBL5,SETUP
.MCALL .\$TYPE,,\$TYPDEC,ERRDF,BGNTST,ENDTST,BGNMOD,ENDMOD,CKLOOP
.MCALL .HEADER,.\$SETUP,.\$TRAP,BGNSUB,ENDSUB,.\$ACT11,.\$APTHDR
.MCALL .\$ATYPE,.\$ERROR,.\$TYPOCT,.\$READ.TITLE KDJ11-A CPU DIAGNOSTIC
;*COPYRIGHT (C) OCTOBER,1983
;*DIGITAL EQUIPMENT CORP.
;*MAYNARD, MASS. 01754
;*;*
;*
;*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
;*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
;*;*
\$TN=1
\$SWR=160000 ;:HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT


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214 .TITLE GLOBAL AREAS
215 .SBTTL GLOBAL EQUATES SECTION
216
217 ;**
218 ; THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
219 ; ARE USED IN MORE THAN ONE TEST.
220 ;--
221 .SBTTL BASIC DEFINITIONS
222
223 ;*INITIAL ADDRESS OF THE STACK POINTER *** 1000 ***
224 001000 STACK= 1000
225 .EQUIV EMT,ERROR ;:BASIC DEFINITION OF ERROR CALL
226 .EQUIV IOT,SCOPE ;:BASIC DEFINITION OF SCOPE CALL
227
228 ;*MISCELLANEOUS DEFINITIONS
229 000011 HT= 11 ;:CODE FOR HORIZONTAL TAB
230 000012 LF= 12 ;:CODE FOR LINE FEED
231 000015 CR= 15 ;:CODE FOR CARRIAGE RETURN
232 000200 CRLF= 200 ;:CODE FOR CARRIAGE RETURN-LINE FEED
233 177776 PS= 177776 ;:PROCESSOR STATUS WORD
234 .EQUIV PS,PSW
235 177774 STKLMT= 177774 ;:STACK LIMIT REGISTER
236 177772 PIRQ= 177772 ;:PROGRAM INTERRUPT REQUEST REGISTER
237 177570 DSMR= 177570 ;:HARDWARE SWITCH REGISTER
238 177570 DDISP= 177570 ;:HARDWARE DISPLAY REGISTER
239
240 ;*GENERAL PURPOSE REGISTER DEFINITIONS
241 000000 R0= #0 ;:GENERAL REGISTER
242 000001 R1= #1 ;:GENERAL REGISTER
243 000002 R2= #2 ;:GENERAL REGISTER
244 000003 R3= #3 ;:GENERAL REGISTER
245 000004 R4= #4 ;:GENERAL REGISTER
246 000005 R5= #5 ;:GENERAL REGISTER
247 000006 R6= #6 ;:GENERAL REGISTER
248 000007 R7= #7 ;:GENERAL REGISTER
249 000006 SP= #6 ;:STACK POINTER
250 000007 PC= #7 ;:PROGRAM COUNTER
251
252 ;*PRIORITY LEVEL DEFINITIONS
253 000000 PRO= 0 ;:PRIORITY LEVEL 0
254 000040 PR1= 40 ;:PRIORITY LEVEL 1
255 000100 PR2= 100 ;:PRIORITY LEVEL 2
256 000140 PR3= 140 ;:PRIORITY LEVEL 3
257 000200 PR4= 200 ;:PRIORITY LEVEL 4
258 000240 PR5= 240 ;:PRIORITY LEVEL 5
259 000300 PR6= 300 ;:PRIORITY LEVEL 6
260 000340 PR7= 340 ;:PRIORITY LEVEL 7
261
262 ;*"SWITCH REGISTER" SWITCH DEFINITIONS
263 100000 SW15= 100000
264 040000 SW14= 40000
265 020000 SW13= 20000
266 010000 SW12= 10000
267 004000 SW11= 4000
268 002000 SW10= 2000
269 001000 SW09= 1000

```


GLOBAL AREAS MACY11 30A(1052) 15-MAR-84 13:28 PAGE 8
 KDJ11A.MAC 22-FEB-84 15:12 BASIC DEFINITIONS

270	000400	SW08=	400
271	000200	SW07=	200
272	000100	SW06=	100
273	000040	SW05=	40
274	000020	SW04=	20
275	000010	SW03=	10
276	000004	SW02=	4
277	000002	SW01=	2
278	000001	SW00=	1
279		.EQUIV	SW09,SW9
280		.EQUIV	SW08,SW8
281		.EQUIV	SW07,SW7
282		.EQUIV	SW06,SW6
283		.EQUIV	SW05,SW5
284		.EQUIV	SW04,SW4
285		.EQUIV	SW03,SW3
286		.EQUIV	SW02,SW2
287		.EQUIV	SW01,SW1
288		.EQUIV	SW00,SW0
289			
290		;*DATA BIT DEFINITIONS (BIT00 TO BIT15)	
291	100000	BIT15=	100000
292	040000	BIT14=	40000
293	020000	BIT13=	20000
294	010000	BIT12=	10000
295	004000	BIT11=	4000
296	002000	BIT10=	2000
297	001000	BIT09=	1000
298	000400	BIT08=	400
299	000200	BIT07=	200
300	000100	BIT06=	100
301	000040	BIT05=	40
302	000020	BIT04=	20
303	000010	BIT03=	10
304	000004	BIT02=	4
305	000002	BIT01=	2
306	000001	BIT00=	1
307		.EQUIV	BIT09,BIT9
308		.EQUIV	BIT08,BIT8
309		.EQUIV	BIT07,BIT7
310		.EQUIV	BIT06,BIT6
311		.EQUIV	BIT05,BIT5
312		.EQUIV	BIT04,BIT4
313		.EQUIV	BIT03,BIT3
314		.EQUIV	BIT02,BIT2
315		.EQUIV	BIT01,BIT1
316		.EQUIV	BIT00,BIT0
317			
318		;*BASIC "CPU" TRAP VECTOR ADDRESSES	
319	000004	ERRVEC=	4
320	000010	RESVEC=	10
321	000014	TBITVEC=	14
322	000014	TRTVEC=	14
323	J00014	BPTVEC=	14
324	000020	IOTVEC=	20
325	000024	PWRVEC=	24

;; TIME OUT AND OTHER ERRORS
 ;; RESERVED AND ILLEGAL INSTRUCTIONS
 ;; "T" BIT
 ;; TRACE TRAP
 ;; BREAKPOINT TRAP (BPT)
 ;; INPUT/OUTPUT TRAP (IOT) **SCOPE**
 ;; POWER FAIL

326	000030	EMTVEC= 30	:: EMULATOR TRAP (EMT) **ERROR**
327	000034	TRAPVEC=34	:: "TRAP" TRAP
328	000060	TKVEC= 60	:: TTY KEYBOARD VECTOR
329	000064	TPVEC= 64	:: TTY PRINTER VECTOR
330	000240	PIRQVEC=240	:: PROGRAM INTERRUPT REQUEST VECTOR
331		.SBTTL	MEMORY MANAGEMENT DEFINITIONS
332			
333		;*KT11 VECTOR ADDRESS	
334			
335	000250	MMVEC= 250	
336			
337		;*KT11 STATUS REGISTER ADDRESSES	
338			
339	177572	SR0= 177572	
340	177574	SR1= 177574	
341	177576	SR2= 177576	
342	172516	SR3= 172516	
343			
344		;*USER "I" PAGE DESCRIPTOR REGISTERS	
345			
346	177600	UIPDR0= 177600	
347	177602	UIPDR1= 177602	
348	177604	UIPDR2= 177604	
349	177606	UIPDR3= 177606	
350	177610	UIPDR4= 177610	
351	177612	UIPDR5= 177612	
352	177614	UIPDR6= 177614	
353	177616	UIPDR7= 177616	
354			
355		;*USER "D" PAGE DESCRIPTOR REGISTERS	
356			
357	177620	UDPDR0= 177620	
358	177622	UDPDR1= 177622	
359	177624	UDPDR2= 177624	
360	177626	UDPDR3= 177626	
361	177630	UDPDR4= 177630	
362	177632	UDPDR5= 177632	
363	177634	UDPDR6= 177634	
364	177636	UDPDR7= 177636	
365			
366		;*USER "I" PAGE ADDRESS REGISTERS	
367			
368	177640	UIPAR0= 177640	
369	177642	UIPAR1= 177642	
370	177644	UIPAR2= 177644	
371	177646	UIPAR3= 177646	
372	177650	UIPAR4= 177650	
373	177652	UIPAR5= 177652	
374	177654	UIPAR6= 177654	
375	177656	UIPAR7= 177656	
376			
377		;*USER "D" PAGE ADDRESS REGISTERS	
378			
379	177660	UDPAR0= 177660	
380	177662	UDPAR1= 177662	
381	177664	UDPAR2= 177664	

382	177666	UDPAR3= 177666
383	177670	UDPAR4= 177670
384	177672	UDPAR5= 177672
385	177674	UDPAR6= 177674
386	177676	UDPAR7= 177676
387		
388		;*SUPERVISOR "I" PAGE DESCRIPTOR REGISTERS
389		
390	172200	SIPDR0= 172200
391	172202	SIPDR1= 172202
392	172204	SIPDR2= 172204
393	172206	SIPDR3= 172206
394	172210	SIPDR4= 172210
395	172212	SIPDR5= 172212
396	172214	SIPDR6= 172214
397	172216	SIPDR7= 172216
398		
399		;*SUPERVISOR "D" PAGE DESCRIPTOR REGISTERS
400		
401	172220	SDPDR0= 172220
402	172222	SDPDR1= 172222
403	172224	SDPDR2= 172224
404	172226	SDPDR3= 172226
405	172230	SDPDR4= 172230
406	172232	SDPDR5= 172232
407	172234	SDPDR6= 172234
408	172236	SDPDR7= 172236
409		
410		;*SUPERVISOR "I" PAGE ADDRESS REGISTERS
411		
412	172240	SIPAR0= 172240
413	172242	SIPAR1= 172242
414	172244	SIPAR2= 172244
415	172246	SIPAR3= 172246
416	172250	SIPAR4= 172250
417	172252	SIPAR5= 172252
418	172254	SIPAR6= 172254
419	172256	SIPAR7= 172256
420		
421		;*SUPERVISOR "D" PAGE ADDRESS REGISTERS
422		
423	172260	SDPAR0= 172260
424	172262	SDPAR1= 172262
425	172264	SDPAR2= 172264
426	172266	SDPAR3= 172266
427	172270	SDPAR4= 172270
428	172272	SDPAR5= 172272
429	172274	SDPAR6= 172274
430	172276	SDPAR7= 172276
431		
432		;*KERNEL "I" PAGE DESCRIPTOR REGISTERS
433		
434	172300	KIPDR0= 172300
435	172302	KIPDR1= 172302
436	172304	KIPDR2= 172304
437	172306	KIPDR3= 172306


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438      172310      KIPDR4= 172310
439      172312      KIPDR5= 172312
440      172314      KIPDR6= 172314
441      172316      KIPDR7= 172316
442
443      ;*KERNEL "D" PAGE DESCRIPTOR REGISTERS
444
445      172320      KDPDR0= 172320
446      172322      KDPDR1= 172322
447      172324      KDPDR2= 172324
448      172326      KDPDR3= 172326
449      172330      KDPDR4= 172330
450      172332      KDPDR5= 172332
451      172334      KDPDR6= 172334
452      172336      KDPDR7= 172336
453
454      ;*KERNEL "I" PAGE ADDRESS REGISTERS
455
456      172340      KIPAR0= 172340
457      172342      KIPAR1= 172342
458      172344      KIPAR2= 172344
459      172346      KIPAR3= 172346
460      172350      KIPAR4= 172350
461      172352      KIPAR5= 172352
462      172354      KIPAR6= 172354
463      172356      KIPAR7= 172356
464
465      ;*KERNEL "D" PAGE ADDRESS REGISTERS
466
467      172360      KDPAR0= 172360
468      172362      KDPAR1= 172362
469      172364      KDPAR2= 172364
470      172366      KDPAR3= 172366
471      172370      KDPAR4= 172370
472      172372      KDPAR5= 172372
473      172374      KDPAR6= 172374
474      172376      KDPAR7= 172376
475
476      ;THESE ARE FLOATING POINT ACCUMULATOR EQUATES
477      000000      AC0=    #0
478      000001      AC1=    #1
479      000002      AC2=    #2
480      000003      AC3=    #3
481      000004      AC4=    #4
482      000005      AC5=    #5
483      000006      AC6=    #6
484      000007      AC7=    #7
485
486      000244      FPVEC=  244
487
488      ;THESE ARE CACHE REGISTER EQUATES
489      177746      CCR=    177746      ;CACHE CONTROL REGISTER
490      177744      MSER=   177744      ;MEMORY SYSTEM ERROR REGISTER
491      177752      HITMIS= 177752      ;HIT/MISS REGISTER
492      177766      CPereg= 177766      ;CPU ERROR REGISTER
493

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494                                     ;MISCELANEOUS DEFINITIONS
495      177546      BEVENT= 177546      ;BEVENT CONTROL REGISTER
496      177560      RCSR= 177560
497      177562      RBUF= 177562
498      177564      XCSR= 177564
499      177566      XBUF= 177566
500      000000      ERRTN= HALT
501      000001      $TSTNU=1
502      000001      ERRNUM= 1      ;INITIALIZE ERROR NUMBER COUNTER
503      002000      AUSWR= 2000      ;SWR FOR APT--NO BEVENT TESTING
504
505
506      ;THIS EQUATE DEFINES THE BOTTOM OF THE PROGRAM STACK POINTER
507      001000      STBOT= 1000
508      000000      .ASECT
509      .SBTTL TRAP CATCHER
510
511      000000      .=0
512      ;*ALL UNUSED LOCATIONS OF THE VECTOR AREA CONTAIN
513      ;*A ".+2, IOT" SEQUENCE TO CATCH AND PROCESS ILLEGAL
514      ;*TRAPS AND INTERRUPTS THAT MIGHT OCCUR.
515      ;*THE IOT TRAP WHICH IS TAKEN ON THE ILLEGAL TRAP/INT
516      ;*TRAPS TO THE $SCOPE ROUTINE WHICH (IF THE RETURN PC IS
517      ;*LESS THAN 1002) JUMPS TO THE $ERROR ROUTINE.
518      ;*THE $ERROR ROUTINE WILL REPORT THE ERROR AS FOLLOWS:
519      ;* PC=YYYYYY UNEXPECTED TRAP TO XXX
520      ;*AND RETURN TO THE PROGRAM AT PC=YYYYYY+2
521      ;*WHERE XXX=LOCATION OF ILLEGAL TRAP
522      ;* YYYYYY=PC AT TIME OF TRAP
523      ;*NOTE: IF THE PROCESSOR IS NOT AN 11/05 THE PROGRAM
524      ;* CAN BE STARTED AT ADDRESS 0 AS WELL AS ADDRESS 200.
525
526      000000      000000      $40CAT: HALT      ;;HALT
527      000002      000737      BR      .-100      ;;BRANCH TO 177700 & TIME OUT (NOT ON
528                                     ;;11/05)
529      000004      001266      .WORD      START      ;;VECTOR TO STARTING ADDRESS
530      000006      000340      .WORD      340      ;;WITH PRIORITY LEVEL 7
531                                     .=174
532      000174      000000      DISPREG: .WORD      0      ;;SOFTWARE DISPLAY REGISTER
533      000176      000000      SWREG: .WORD      0      ;;SOFTWARE SWITCH REGISTER
534      .SBTTL STARTING ADDRES(ES)
535      000200      000137      001266      JMP      $START ;;GO TO START OF PROGRAM
536      .SBTTL ACT11 HOOKS
537
538      ;*****
539      ;HOOKS REQUIRED BY ACT11
540      000204      $SVPC=      ;SAVE PC
541      000046      .=46
542      000046      042016      $ENDAD      ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .SEOP
543      000052      000052      .=52
544      000052      000000      .WORD      0      ;;2)SET LOC.52 TO ZERO
545      000204      .=$SVPC      ;; RESTORE PC
546      .SBTTL APT PARAMETER BLOCK
547
548      ;*****
549      ;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT

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001006 000000
001010 000000
001012 000000
001014 000000
001016 000000
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001021 000
001022 000000
001024 002000
001026 000000

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001046 177570
001050 177570
001052 000000

001054 000000
001056 000000
001060 000000
001062 000000
001064 000000

.SBTTL GLOBAL DATA SECTION

; THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
; IN MORE THAN ONE TEST.

.SBTTL APT MAILBOX-ETABLE

; .EVEN
\$MAIL: ; APT MAILBOX
\$MSGTY: .WORD AMSGTY ; MESSAGE TYPE CODE
\$FATAL: .WORD AFATAL ; FATAL ERROR NUMBER
\$TESTN: .WORD ATESTN ; TEST NUMBER
\$PASS: .WORD APASS ; PASS COUNT
\$DEVCT: .WORD ADEVCT ; DEVICE COUNT
\$UNIT: .WORD AUNIT ; I/O UNIT NUMBER
\$MSGAD: .WORD AMSGAD ; MESSAGE ADDRESS
\$MSGLG: .WORD AMSGLG ; MESSAGE LENGTH
\$ETABLE: ; APT ENVIRONMENT TABLE
\$ENV: .BYTE AENV ; ENVIRONMENT BYTE
\$ENVH: .BYTE AENVH ; ENVIRONMENT MODE BITS
\$SMREG: .WORD ASMREG ; APT SWITCH REGISTER
\$USMR: .WORD AUSMR ; USER SWITCHES
\$CPUOP: .WORD ACPUOP ; CPU TYPE, OPTIONS
; BITS 15-11-CPU TYPE
; 11/04-01,11/05-02,11/20-03,11/40-04,11/45-05
; 11/70-06,PDQ-07,Q-10
; BIT 10-REAL TIME CLOCK
; BIT 9-FLOATING POINT PROCESSOR
; BIT 8-MEMORY MANAGEMENT
\$ETEND:
.MEXIT

; THESE LOCATIONS ARE USED IN MORE THAN ONE TEST TO STORE VECTOR DATA
; WHEN THE TEST NEEDS TO HAVE AN ERROR CONDITION RESPOND DIFFERENTLY
; FROM THE DEFAULT RESPONSE.

SLOC00: .WORD 0
SLOC01: .WORD 0

; THESE LOCATIONS ARE USED IN MORE THAN ONE TEST TO STORE WORKING DATA.
EXPDAT: .WORD 0 ; STORES EXPECTED (GOOD) DATA FOR COMPARISONS
RECDAT: .WORD 0 ; STORES RECIEVED DATA TO BE VERIFIED
COUNT: .WORD 0 ; ERROR INDICATOR FOR FLOATING POINT TESTS
FLAG: .WORD 0 ; USED TO STORE "FLAG" CONDITIONS
ERRCNT: .WORD 0 ; STORAGE FOR ERROR COUNT
SWR: .WORD DSWR ; STORAGE FOR SWITCH REGISTER ADDRESS
DISPLAY: .WORD DDISP ; STORAGE FOR DISPLAY REGISTER ADDRESS
\$ERFLG: .WORD 0 ; ERROR FLAG

; THESE LOCATIONS ARE USED BY MORE THAN ONE TEST AS LOOP COUNTERS

DCOUNT: .WORD 0
ALLCTR: .WORD 0
LOOPIN: .WORD 0
SAVSP1: .WORD 0
SAVSP2: .WORD 0

; STORAGE FOR UNEXPECTED TRAP DATA
; " " " "

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645

001066 000000
001070 000000
001072 000000

001074 177777

001076
001076 000002

SEQ: .WORD 0
SPS: .WORD 0
SPSJ: .WORD 0

;STORES SEQUENCE NUMBER FOR JUMP TESTS
;STORES STACK POINTER FOR JUMP TESTS
;STORES STACK POINTER FOR JUMP TESTS

WAITIN: .WORD 177777

!!!!!!THIS IS IT. THE PROGRAM TEST LOCATION AND WRITE BUFFER!!!!!!!!!!!!!!!!!!!!!!

TSTLOC:
.BLKW 2


```

646
647      .SBTTL  GLOBAL TEXT SECTION
648
649      ;**
650      ; THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
651      ; MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
652      ; MORE THAN ONE TEST.
653      ;--
654
655      ;
656      ; FORMAT STATEMENTS USED IN PRINT CALLS
657      ;
658      001102 005015 040503 044103 ERRMSG: .ASCIZ <CR><LF>/CACHE SYSTEM ERROR/
659      001110 020105 054523 052123
660      001116 046505 042440 051122
661      001124 051117      000
662      001127      015 042412 051122 CPUERR: .ASCIZ <CR><LF>/ERROR DURING CPU TESTS/
663      001134 051117 042040 051125
664      001142 047111 020107 050103
665      001150 020125 042524 052123
666      001156 000123
667      001160 005015 051105 047522 BRDERR: .ASCIZ <CR><LF>/ERROR WHILE TESTING BOARD FUNCTIONS/
668      001166 020122 044127 046111
669      001174 020105 042524 052123
670      001202 047111 020107 047502
671      001210 051101 020104 052506
672      001216 041516 044524 047117
673      001224 000123
674      001226 005015 051105 047522 ERR1: .ASCIZ <CR><LF>/ERROR # =/
675      001234 020122 020043 000075
676      001242 005015 051105 047522 ERR2: .ASCIZ <CR><LF>/ERROR PC =/
677      001250 020122 041520 036440
678      001256      000
679      001257      015 020012 020040 %CRLF: .ASCIZ <CR><LF>/ /
680      001264      000
681      001266      .EVEN

```

GLOBAL AREAS
KDJ11A.MAC

MACY11 30A(1052)
22-FEB-84 15:12

15-MAR-84 13:28 PAGE 17

GLOBAL ERROR REPORT SECTION

SEQ 0017

682
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688

.SBTTL GLOBAL ERROR REPORT SECTION

;++

: THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
: USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION.

--

GLOBAL AREAS
KDJ11A.MAC

MACY11 30A(1052)
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GLOBAL SUBROUTINES SECTION

SEQ 0018

689
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.SBTTL GLOBAL SUBROUTINES SECTION

!++
! THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
! THAT ARE USED IN MORE THAN ONE TEST.
!--

```

695 001266          START:
696 001266 012737 000014 177746  MOV    #14,#@CCR          ;SET CACHE TO FORCE MISS
697                                     .SBTTL INITIALIZE THE COMMON TAGS
698 001274 012706 001000          MOV    @STACK,SP        ;SETUP THE STACK POINTER
699                                     ;;INITIALIZE A FEW VECTORS
700 001300 012737 043470 000030  MOV    @#ERROR,@#EMTVEC ;;EMT VECTOR FOR ERROR ROUTINE
701 001306 012737 000340 000032  MOV    #340,@#EMTVEC+2 ;;LEVEL 7
702 001314 012737 043152 000034  MOV    @#TRAP,@#TRAPVEC ;;TRAP VECTOR FOR TRAP CALLS
703 001322 012737 000340 000036  MOV    #340,@#TRAPVEC+2;LEVEL 7
704 001330 005067 177452          CLR    #PASS           ;CLEAR THE PASS COUNT
705 001334 016767 040424 040414  MOV    #ENDCT,#EOPCT   ;SETUP END-OF-PROGRAM COUNTER
706 001342 105067 177504          CLR    #ERFLG         ;CLEAR THE ERROR FLAG
707                                     ;;SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
708                                     ;;EQUAL TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.
709 001346 013746 000004          MOV    @#ERRVEC,-(SP)  ;SAVE ERROR VECTOR
710 001352 012737 001406 000004  MOV    #64,@#ERRVEC   ;SET UP ERROR VECTOR
711 001360 012767 177570 177460  MOV    @DSWR,SWR       ;SETUP FOR A HARDWARE SWICH REGISTER
712 001366 012767 177570 177454  MOV    @DDISP,DISPLAY  ;AND A HARDWARE DISPLAY REGISTER
713 001374 022777 177777 177444  CMP    #-1,@SWR        ;TRY TO REFERENCE HARDWARE SWR
714 001402 001012          BNE    66#            ;BRANCH IF NO TIMEOUT TRAP OCCURRED
715                                     ;AND THE HARDWARE SWR IS NOT = -1
716 001404 000403          BR     65#            ;BRANCH IF NO TIMEOUT
717 001406 012716 001414          64#:  MOV    #65#,(SP)   ;SET UP FOR TRAP RETURN
718 001412 000002          RTI
719 001414 012767 000176 177424  65#:  MOV    @SWREG,SWR    ;POINT TO SOFTWARE SWR
720 001422 012767 000174 177420  MOV    @DISPREG,DISPLAY
721 001430 012637 000004          66#:  MOV    (SP)+,@#ERRVEC ;RESTORE ERROR VECTOR
722
723                                     .MACRO  ##SETHAIL      ?#ARG1
724                                     CLR    #PASS           ;CLEAR PASS COUNT
725                                     BITB   @APTSIZE,#ENVM   ;TEST USER SIZE UNDER APT
726                                     BEQ    #ARG1            ;YES,USE NON-APT SWITCH
727                                     MOV    @#SWREG,SWR     ;NO,USE APT SWITCH REGISTER
728                                     #ARG1:
729                                     .ENDM
730 001434 005067 177346          ##SETHAIL
731 001440 132767 000200 177353  CLR    #PASS           ;CLEAR PASS COUNT
732 001446 001403          BITB   @APTSIZE,#ENVM ;TEST USER SIZE UNDER APT
733 001450 012767 001022 177370  BEQ    67#            ;YES,USE NON-APT SWITCH
734 001456          MOV    @#SWREG,SWR     ;NO,USE APT SWITCH REGISTER
735 001456 012737 043470 000020  67#:  MOV    @#ERROR,@#IOTVEC ;SET UP IOT VECTORS
736 001464 012737 000340 000022  MOV    #340,@#IOTVEC+2 ;TO GO TO ERROR ROUTINE
737 001472 005037 177766          CLR    #177766        ;CLEAR CPU ERROR REGISTER
738 001476 005067 177302          RESTART: CLR #TESTN    ;RESET #TESTN TO ZERO
739 001502 012737 000014 177746  MOV    #14,@#CCR      ;SET CACHE TO FORCE MISS
740
741                                     .SBTTL BASE INSTRUCTION SET TESTS
742                                     ;*****
743                                     ;*****
744                                     ;
745                                     ;           BEGIN BASE INSTRUCTION SET TESTING
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753 001510
754 001510 005267 177270
755 001514 000277
756 001516 000244
757 001520 001401
758 001522 001003
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764 001524
765 001524 104000
766 001526 000001
767 001530 001127
768 001532 000257
769 001534 000264
770 001536 001001
771 001540 001403
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773 001542
774 001542 104000
775 001544 000002
776 001546 001127
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786 001550 005267 177230
787 001554 000257
788 001556 103003
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791 001560 104000
792 001562 000003
793 001564 001127
794 001566 000261
795 001570 103403
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797 001572
798 001572 104000
799 001574 000004
800 001576 001127
801 001600
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803 001600
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;THESE TWO INSTRUCTIONS ARE FUNDAMENTAL TO RECOGNIZING ERROR CONDITIONS
;*****

```

```

TST1:
      INC      $TESTN      ;INCREMENT TEST NUMBER
      SCC
      CLZ
      BEQ      1$
      BNE      2$
;CC=0100 - Z BIT CLEARED
;*TEST INSTR -TRY TO CAUSE A BEQ ERROR
;BRANCH IF GOOD
;THE Z FLAG DIDNT CLEAR OR BRANCH FAILED.
;FAILURE AT THIS LOCATION
;COULD MEAN A BUS PROBLEM, MICRO-CODE PROBLEM
;CONDITION CODE PROBLEM OR JUST ABOUT ANYTHING
;ELSE.

1$:
      ERROR
      .WORD    1           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR     ;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

2$:
      CCC
      SEZ
      BNE      3$
      BEQ      4$
;COND CODES = 0100 (ZERO)
;*TEST INSTR* TRY TO BRANCH ON ZERO FLAG
;*TEST INSTR* BRANCH IF GOOD
;BRANCH FAILURE WITH Z BIT SET

3$:
      ERROR
      .WORD    2           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR     ;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

4$:

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M2:
;*****
;*TEST 2      TEST BRANCH ON CARRY
;*****
;THIS IS A TEST TO SEE IF THE MODULE FORM ANTICIPATED IS FEASIBLE.
;*****

```

```

TST2:
      INC      $TESTN      ;INCREMENT TEST NUMBER
      CCC
      BCC      2$
;*TEST INSTR*
;BRANCH CARRY CLEAR FAILED

1$:
      ERROR
      .WORD    3           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR     ;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

2$:
      SEC
      BCS      4$
;CC=1111
;*TEST INSTR*
; BRANCH CARRY SET FAILED

3$:
      ERROR
      .WORD    4           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR     ;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

4$:

```

```

M3:
;*****
;*TEST 3      TEST DATA PATHS
;*****

```



```

863 001710 005267 177070      INC      $TESTN      ;INCREMENT TEST NUMBER
864 001714 005037 000000      CLR      0#0         ;
865 001720 005137 000000      COM      0#0         ;SET UP MEMORY LOCATION 0 = 111111
866 001724 023727 000000 177777  CMP      0#0,#177777 ;TEST DATA
867 001732 001403              BEQ      2#          ;BRANCH IF NO ERROR
868 001734              1#:
869 001734 104000              ERROR
870 001736 000010              .WORD   10          ;ALL ERRORS TO TRAP TO EMT VECTOR
871 001740 001127              .WORD   CPUERR      ;UNIQUE ERROR NUMBER
872 001742              2#:
873
874
875 001742              ;
876              ;GPROTS:
877              ;*****
878              ;*TEST 7      RO BIT TESTS
879              ;*****
880 001742 005267 177036      TST7:
881 001746 012700 177777      INC      $TESTN      ;INCREMENT TEST NUMBER
882 001752 020027 177777      MOV      #177777,R0  ;RO=177777
883 001756 001403              CMP      R0,#177777 ;DOES RO=177777
884              BEQ      1#          ;YES GO ON
885              ;NO GO TO ERROR
886 001760 104000              ERROR
887 001762 000011              .WORD   11          ;ALL ERRORS TO TRAP TO EMT VECTOR
888 001764 001127              .WORD   CPUERR      ;UNIQUE ERROR NUMBER
889 001770 020027 000000 1#:      CLR      R0          ;ADDRESS OF ERROR MESSAGE
890 001774 001403              CMP      R0,#0       ;RO=0
891              BEQ      2#          ;DOES RO=0
892              ;YES GO ON
893              ;NO GO TO ERROR
894 001776 104000              ERROR
895 002000 000012              .WORD   12          ;ALL ERRORS TO TRAP TO EMT VECTOR
896 002002 001127              .WORD   CPUERR      ;UNIQUE ERROR NUMBER
897 002004 012700 125252 2#:      MOV      #125252,R0 ;ADDRESS OF ERROR MESSAGE
898 002010 020027 125252      CMP      R0,#125252 ;RO=125252
899 002014 001403              BEQ      3#          ;DOES RO=125252
900              ;YES GO ON
901              ;NO GO TO ERROR
902 002016 104000              ERROR
903 002020 000013              .WORD   13          ;ALL ERRORS TO TRAP TO EMT VECTOR
904 002022 001127              .WORD   CPUERR      ;UNIQUE ERROR NUMBER
905 002024 012700 052525 3#:      MOV      #52525,R0  ;ADDRESS OF ERROR MESSAGE
906 002030 020027 052525      CMP      R0,#52525  ;RO=52525
907 002034 001403              BEQ      4#          ;DOES RO=52525
908              ;YES GO ON
909              ;NO GO TO ERROR
910 002036 104000              ERROR
911 002040 000014              .WORD   14          ;ALL ERRORS TO TRAP TO EMT VECTOR
912 002042 001127              .WORD   CPUERR      ;UNIQUE ERROR NUMBER
913              4#:
914              ;
915              ;GPR1TS:
916              ;*****
917              ;*TEST 10     R1 BIT TESTS
918              ;*****
919 002044 005267 176734      TST10:
920 002050 012701 177777      INC      $TESTN      ;INCREMENT TEST NUMBER
921              MOV      #177777,R1  ;R1=177777

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919 002054 020127 177777      CMP      R1,#177777      ;DOES R1=177777
920 002060 001403              BEQ      1#              ;YES GO ON
921                                ;NO GO TO ERROR
922 002062 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
923 002064 000015              .WORD    15              ;UNIQUE ERROR NUMBER
924 002066 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
925 002070 005001              1#:     CLR      R1              ;R1=0
926 002072 020127 000000      CMP      R1,#0           ;DOES R1=0
927 002076 001403              BEQ      2#              ;YES GO ON
928                                ;NO GO TO ERROR
929 002100 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
930 002102 000016              .WORD    16              ;UNIQUE ERROR NUMBER
931 002104 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
932 002106 012701 125252      2#:     MOV      #125252,R1 ;R1=125252
933 002112 020127 125252      CMP      R1,#125252     ;DOES R1=125252
934 002116 001403              BEQ      3#              ;YES GO ON
935                                ;NO GO TO ERROR
936 002120 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
937 002122 000017              .WORD    17              ;UNIQUE ERROR NUMBER
938 002124 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
939 002126 012701 052525      3#:     MOV      #52525,R1  ;R1=52525
940 002132 020127 052525      CMP      R1,#52525     ;DOES R1=52525
941 002136 001403              BEQ      4#              ;YES GO ON
942                                ;NO GO TO ERROR
943 002140 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
944 002142 000020              .WORD    20              ;UNIQUE ERROR NUMBER
945 002144 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
946 002146              4#:
947
948
949 002146              ;
950              GPR2TS:
951              ;*****
952              ;*TEST 11      R2 BIT TESTS
953              ;*****
954              TST11:
955 002146 005267 176632      INC      #TESTN          ;INCREMENT TEST NUMBER
956 002152 012702 177777      MOV      #177777,R2     ;R2=177777
957 002156 020227 177777      CMP      R2,#177777     ;DOES R2=177777
958 002162 001403              BEQ      1#              ;YES GO ON
959                                ;NO GO TO ERROR
960 002164 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
961 002166 000021              .WORD    21              ;UNIQUE ERROR NUMBER
962 002170 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
963 002172 005002              1#:     CLR      R2              ;R2=0
964 002174 020227 000000      CMP      R2,#0           ;DOES R2=0
965 002200 001403              BEQ      2#              ;YES GO ON
966                                ;NO GO TO ERROR
967 002202 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
968 002204 000022              .WORD    22              ;UNIQUE ERROR NUMBER
969 002206 001127              .WORD    CPUERR          ;ADDRESS OF ERROR MESSAGE
970 002210 012702 125252      2#:     MOV      #125252,R2 ;R2=125252
971 002214 020227 125252      CMP      R2,#125252     ;DOES R2=125252
972 002220 001403              BEQ      3#              ;YES GO ON
973                                ;NO GO TO ERROR
974 002222 104000              ERROR     ;ALL ERRORS TO TRAP TO EMT VECTOR
975 002224 000023              .WORD    23              ;UNIQUE ERROR NUMBER

```



```

975 002226 001127
976 002230 012702 052525
977 002234 020227 052525
978 002240 001403
979
980 002242 104000
981 002244 000024
982 002246 001127
983 002250
984
985
986 002250
987
988
989
990 002250
991 002250 005267 176530
992 002254 012703 177777
993 002260 020327 177777
994 002264 001403
995
996 002266 104000
997 002270 000025
998 002272 001127
999 002274 005003
1000 002276 020327 000000
1001 002302 001403
1002
1003 002304 104000
1004 002306 000026
1005 002310 001127
1006 002312 012703 125252
1007 002316 020327 125252
1008 002322 001403
1009
1010 002324 104000
1011 002326 000027
1012 002330 001127
1013 002332 012703 052525
1014 002336 020327 052525
1015 002342 001403
1016
1017 002344 104000
1018 002346 000030
1019 002350 001127
1020 002352
1021
1022
1023 002352
1024
1025
1026
1027 002352
1028 002352 005267 176426
1029 002356 012704 177777
1030 002362 020427 177777

;
;*****
;GPR3TS:
;*****
;*TEST 12 R3 BIT TESTS
;*****
TST12:
INC $TESTN ;INCREMENT TEST NUMBER
MOV #177777,R3 ;R3=177777
CMP R3,#177777 ;DOES R3=177777
BEQ 1$ ;YES GO ON
;NO GO TO ERROR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R3=0
1$: CLR R3 ;DOES R3=0
CMP R3,#0 ;YES GO ON
;NO GO TO ERROR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
2$: MOV #125252,R3 ;R3=125252
CMP R3,#125252 ;DOES R3=125252
BEQ 3$ ;YES GO ON
;NO GO TO ERROR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
3$: MOV #52525,R3 ;R3=52525
CMP R3,#52525 ;DOES R3=52525
BEQ 4$ ;YES GO ON
;NO GO TO ERROR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
4$:

;
;GPR4TS:
;*****
;*TEST 13 R4 BIT TESTS
;*****
TST13:
INC $TESTN ;INCREMENT TEST NUMBER
MOV #177777,R4 ;R4=177777
CMP R4,#177777 ;DOES R4=177777

```

```

1031 002366 001403          BEQ      1#          ;YES GO ON
1032                                ;NO GO TO ERROR
1033 002370 104000          ERROR
1034 002372 000031          .WORD   31          ;ALL ERRORS TO TRAP TO EMT VECTOR
1035 002374 001127          .WORD   CPUERR      ;UNIQUE ERROR NUMBER
1036 002376 005004          CLR      R4          ;ADDRESS OF ERROR MESSAGE
1037 002400 020427 000000 1#:    CMP      R4,#0      ;R4=0
1038 002404 001403          BEQ      2#          ;DOES R4=0
1039                                ;YES GO ON
1040                                ;NO GO TO ERROR
1040 002406 104000          ERROR
1041 002410 000032          .WORD   32          ;ALL ERRORS TO TRAP TO EMT VECTOR
1042 002412 001127          .WORD   CPUERR      ;UNIQUE ERROR NUMBER
1043 002414 012704 125252 2#:    MOV      #125252,R4 ;ADDRESS OF ERROR MESSAGE
1044 002420 020427 125252          CMP      R4,#125252 ;R4=125252
1045 002424 001403          BEQ      3#          ;DOES R4=125252
1046                                ;YES GO ON
1047 002426 104000          ERROR
1048 002430 000033          .WORD   33          ;NO GO TO ERROR
1049 002432 001127          .WORD   CPUERR      ;ALL ERRORS TO TRAP TO EMT VECTOR
1050 002434 012704 052525 3#:    MOV      #52525,R4 ;UNIQUE ERROR NUMBER
1051 002440 020427 052525          CMP      R4,#52525 ;ADDRESS OF ERROR MESSAGE
1052 002444 001403          BEQ      4#          ;R4=52525
1053                                ;DOES R4=52525
1054 002446 104000          ERROR
1055 002450 000034          .WORD   34          ;YES GO ON
1056 002452 001127          .WORD   CPUERR      ;NO GO TO ERROR
1057 002454          ;ALL ERRORS TO TRAP TO EMT VECTOR
1058                                ;UNIQUE ERROR NUMBER
1059                                ;ADDRESS OF ERROR MESSAGE
1060 002454          ;
1061          ;GPRSTS:
1062          ;*****
1063          ;*TEST 14      R5 BIT TESTS
1064          ;*****
1064 002454          TST14:
1065 002454 005267 176324          INC      #TESTN      ;INCREMENT TEST NUMBER
1066 002460 012705 177777          MOV      #177777,R5 ;R5=177777
1067 002464 020527 177777          CMP      R5,#177777 ;DOES R5=177777
1068 002470 001403          BEQ      1#          ;YES GO ON
1069                                ;NO GO TO ERROR
1070                                ;ALL ERRORS TO TRAP TO EMT VECTOR
1070 002472 104000          ERROR
1071 002474 000035          .WORD   35          ;UNIQUE ERROR NUMBER
1072 002476 001127          .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
1073 002500 005005          CLR      R5          ;R5=0
1074 002502 020527 000000 1#:    CMP      R5,#0      ;DOES R5=0
1075 002506 001403          BEQ      2#          ;YES GO ON
1076                                ;NO GO TO ERROR
1077                                ;ALL ERRORS TO TRAP TO EMT VECTOR
1077 002510 104000          ERROR
1078 002512 000036          .WORD   36          ;UNIQUE ERROR NUMBER
1079 002514 001127          .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
1080 002516 012705 125252 2#:    MOV      #125252,R5 ;R5=125252
1081 002522 020527 125252          CMP      R5,#125252 ;DOES R5=125252
1082 002526 001403          BEQ      3#          ;YES GO ON
1083                                ;NO GO TO ERROR
1084                                ;ALL ERRORS TO TRAP TO EMT VECTOR
1084 002530 104000          ERROR
1085 002532 000037          .WORD   37          ;UNIQUE ERROR NUMBER
1086 002534 001127          .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
    
```



```

1087 002536 012705 052525      3$:  MOV    #52525,R5      ;R5=52525
1088 002542 020527 052525      CMP    R5,#52525      ;DOES R5=52525
1089 002546 001403              BEQ    4$              ;YES GO ON
1090                                ;NO GO TO ERROR
1091 002550 104000              ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
1092 002552 000040              .WORD  40              ;UNIQUE ERROR NUMBER
1093 002554 001127              .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
1094 002556
1095
1096
1097 002556      ;
1098      ;GPR6TS:
1099      ;*****
1100      ;*TEST 15      R6 BIT TESTS
1101      ;*****
1101 002556      TST15:
1102 002556 005267 176222      INC    #TESTN          ;INCREMENT TEST NUMBER
1103 002562 012706 177777      MOV    #177777,R6     ;R6=177777
1104 002566 020627 177777      CMP    R6,#177777     ;DOES R6=177777
1105 002572 001403              BEQ    1$              ;YES GO ON
1106                                ;NO GO TO ERROR
1107 002574 104000              ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
1108 002576 000041              .WORD  41              ;UNIQUE ERROR NUMBER
1109 002600 001127              .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
1110 002602 005006      1$:  CLR    R6              ;R6=0
1111 002604 020627 000000      CMP    R6,#0          ;DOES R6=0
1112 002610 001403              BEQ    2$              ;YES GO ON
1113                                ;NO GO TO ERROR
1114 002612 104000              ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
1115 002614 000042              .WORD  42              ;UNIQUE ERROR NUMBER
1116 002616 001127              .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
1117 002620 012706 125252      2$:  MOV    #125252,R6     ;R6=125252
1118 002624 020627 125252      CMP    R6,#125252     ;DOES R6=125252
1119 002630 001403              BEQ    3$              ;YES GO ON
1120                                ;NO GO TO ERROR
1121 002632 104000              ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
1122 002634 000043              .WORD  43              ;UNIQUE ERROR NUMBER
1123 002636 001127              .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
1124 002640 012706 052525      3$:  MOV    #52525,R6     ;R6=52525
1125 002644 020627 052525      CMP    R6,#52525     ;DOES R6=52525
1126 002650 001403              BEQ    4$              ;YES GO ON
1127                                ;NO GO TO ERROR
1128 002652 104000              ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
1129 002654 000044              .WORD  44              ;UNIQUE ERROR NUMBER
1130 002656 001127              .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
1131 002660 012706 001000      4$:  MOV    #STBOT,R6     ;RESTORE SP
1132
1133
1134 002664      ;
1135      ;PSWBTS:
1136      ;*****
1137      ;*TEST 16      PSW LOW BYTE BIT TESTS
1138      ;*****
1138 002664      TST16:
1139 002664 005267 176114      INC    #TESTN          ;INCREMENT TEST NUMBER
1140 002670 012737 000377 177776      MOV    #377,8#177776 ;PS=357 T BIT SHOULDN'T SET
1141 002676 022737 000357 177776      CMP    #357,8#177776 ;DOES PS=357
1142 002704 001403              BEQ    1$              ;YES GO ON

```

```

1143
1144 002706 104000 ERROR
1145 002710 000045 .WORD 45
1146 002712 001127 .WORD CPUERR
1147 002714 005037 177776 18: CLR 8#177776
1148 002720 022737 000000 177776 CMP #0,8#177776
1149 002726 001403 BEQ 2#
1150
1151 002730 104000 ERROR
1152 002732 000046 .WORD 46
1153 002734 001127 .WORD CPUERR
1154 002736 012737 000105 177776 28: MOV #105,8#177776
1155 002744 022737 000105 177776 CMP #105,8#177776
1156 002752 001403 BEQ 3#
1157
1158 002754 104000 ERROR
1159 002756 000047 .WORD 47
1160 002760 001127 .WORD CPUERR
1161 002762 012737 000252 177776 38: MOV #252,8#177776
1162 002770 022737 000252 177776 CMP #252,8#177776
1163 002776 001403 BEQ 4#
1164
1165 003000 104000 ERROR
1166 003002 000050 .WORD 50
1167 003004 001127 .WORD CPUERR
1168 003006 48:
1169
1170
1171 003006
1172
1173
1174
1175
1176
1177 003006
1178 003006 005267 175772
1179 003012 005004
1180 003014 005104
1181 003016 005004
1182 003020 001403
1183 003022
1184 003022 104000
1185 003024 000051
1186 003026 001127
1187 003030 005104
1188 003032 005204
1189 003034 001403
1190
1191 003036
1192 003036 104000
1193 003040 000052
1194 003042 001127
1195 003044
1196
1197
1198 003044

```

MSPO:

```

;*****
; *TEST 17 TEST SINGLE OPERAND INSTRUCTIONS- MODE 0
;*****
;THE INC, COM, CLR, AND DECREMENT INSTRUCTIONS ARE VERIFIED.
;*****
TST17:
INC #TESTN
CLR R4
COM R4
CLR R4
BEQ 2#
; INCREMENT TEST NUMBER
; INITIALIZE R4 WITH DATA
;
; *TEST INSTRUCTION
; BRANCH IF R4 CLEARED
18:
ERROR
.WORD 51
.WORD CPUERR
28:
COM R4
INC R4
BEQ 4#
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; *TEST COMPLIMENT INSTRUCTION
; *TEST INCREMENT INSTRUCTION
; BRANCH IF R4 =0
; COMPLIMENT OR INCREMENT FAILED
38:
ERROR
.WORD 52
.WORD CPUERR
48:
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; MSPB:

```



```

1199
1200
1201
1202 003044
1203 003044 005267 175734
1204 003050 005004
1205 003052 005104
1206 003054 105004
1207 003056 001403
1208
1209 003060
1210 003060 104000
1211 003062 000053
1212 003064 001127
1213 003066 105304
1214 003070 100002
1215 003072 105104
1216 003074 001403
1217
1218 003076
1219 003076 104000
1220 003100 000054
1221 003102 001127
1222 003104
1223
1224
1225 003104
1226
1227
1228
1229 003104
1230 003104 005267 175674
1231 003110 005004
1232 003112 005014
1233 003114 005114
1234 003116 005014
1235 003120 001403
1236
1237 003122
1238 003122 104000
1239 003124 000055
1240 003126 001127
1241 003130 005114
1242 003132 001403
1243 003134 100002
1244 003136 005214
1245 003140 001403
1246
1247 003142
1248 003142 104000
1249 003144 000056
1250 003146 001127
1251 003150
1252
1253
1254 003150

```

```

;*****
; *TEST 20 TEST SINGLE OPS - EVEN BYTE OF CLRB, DECB, AND COMB
;*****
TST20:
    INC      #TESTN      ;INCREMENT TEST NUMBER
    CLR      R4
    COM      R4          ;SETUP TEST REGISTER
    CLRB     R4          ;*TEST CLEAR BYTE INSTRUCTION
    BEQ      2#         ;BRANCH IF GOOD
                                ;CLEAR EVEN BYTE FAILED
1#:
    ERROR    .WORD      53      ;ALL ERRORS TO TRAP TO EMT VECTOR
    .WORD    CPUERR        ;UNIQUE ERROR NUMBER
    .WORD    CPUERR        ;ADDRESS OF ERROR MESSAGE
2#:
    DECB     R4          ;*TEST DECREMENT BYTE
    BPL      3#         ;DECREMENT BYTE FAILED
    COM      R4          ;*TEST COMPLIMENT BYTE
    BEQ      4#         ;BRANCH IF GOOD
                                ;COMPLIMENT OR DECREMENT FAILED TO WORK
3#:
    ERROR    .WORD      54      ;ALL ERRORS TO TRAP TO EMT VECTOR
    .WORD    CPUERR        ;UNIQUE ERROR NUMBER
    .WORD    CPUERR        ;ADDRESS OF ERROR MESSAGE
4#:
;
;MSPC:
;*****
; *TEST 21 TEST SINGLE OPS - MODE 1 CLRB, COMB, AND INCB
;*****
TST21:
    INC      #TESTN      ;INCREMENT TEST NUMBER
    CLR      R4
    CLR      (R4)
    COM      (R4)        ;SETUP TEST DATA
    CLR      (R4)        ;*TEST INSTRUCTION
    BEQ      2#         ;BRANCH IF GOOD
                                ;MODE 1 FAILED
1#:
    ERROR    .WORD      55      ;ALL ERRORS TO TRAP TO EMT VECTOR
    .WORD    CPUERR        ;UNIQUE ERROR NUMBER
    .WORD    CPUERR        ;ADDRESS OF ERROR MESSAGE
2#:
    COM      (R4)        ;*TEST INSTRUCTION
    BEQ      3#         ;(0)SHOULD = -1
    BPL      3#
    INC      (R4)
    BEQ      4#         ;*TEST INSTRUCTION
                                ;BRANCH IF GOOD
                                ;COM OR INC FAILED TO ALTER LOC 0 CORRECTLY
3#:
    ERROR    .WORD      56      ;ALL ERRORS TO TRAP TO EMT VECTOR
    .WORD    CPUERR        ;UNIQUE ERROR NUMBER
    .WORD    CPUERR        ;ADDRESS OF ERROR MESSAGE
4#:
;
;MSPD:

```

1255
1256
1257
1258 003150
1259 003150 005267 175630
1260 003154 005004
1261 003156 005014
1262 003160 005114
1263 003162 105014
1264 003164 105014
1265 003166 001403
1266
1267 003170
1268 003170 104000
1269 003172 000057
1270 003174 001127
1271 003176 105214
1272 003200 100405
1273 003202 001404
1274 003204 105114
1275 003206 105214
1276 003210 105214
1277 003212 001403
1278
1279 003214
1280 003214 104000
1281 003216 000060
1282 003220 001127
1283 003222
1284
1285
1286 003222
1287
1288
1289
1290 003222
1291 003222 005267 175556
1292 003226 005004
1293 003230 005014
1294 003232 005114
1295 003234 005204
1296 003236 105014
1297 003240 001403
1298
1299 003242 104000
1300 003244 000061
1301 003246 001127
1302 003250 005304
1303 003252 005214
1304 003254 005204
1305 003256 105114
1306 003260 105214
1307 003262 100003
1308 003264 001402
1309 003266 105214
1310 003270 001403

```

*****
;*TEST 22      TEST SINGLE OPS MODE1-EVEN BYTE-CLRB,COMB,INCB
*****
TST22:
      INC      #TESTN          ;INCREMENT TEST NUMBER
      CLR      R4
      CLR      (R4)
      COM      (R4)          ;SETUP TEST DATA
      CLRB     (R4)          ;*TEST INSTRUCTION
      CLRB     (R4)          ;*TEST INSTRUCTION
      BEQ      2#           ;BRANCH IF GOOD
                          ;CLEAR (0) EVEN BYTE FAILED

1# :   ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    57       ;UNIQUE ERROR NUMBER
      .WORD    CPUERR   ;ADDRESS OF ERROR MESSAGE

2# :   INCB      (R4)    ;*TEST INSTRUCTION
      BMI      3#
      BEQ      3#       ; TEST FLAGS
      COMB     (R4)    ;*TEST INSTRUCTION
      INCB     (R4)
      INCB     (R4)
      BEQ      4#
                          ;BRANCH IF GOOD
                          ;COMB OR INCB FAILED

3# :   ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    60       ;UNIQUE ERROR NUMBER
      .WORD    CPUERR   ;ADDRESS OF ERROR MESSAGE

4# :

;MSPEO:
*****
;*TEST 23      TEST SINGLE OPS - ODD BYTE - CLRB, COMB, DECB
*****
TST23:
      INC      #TESTN          ;INCREMENT TEST NUMBER
      CLR      R4
      CLR      (R4)
      COM      (R4)          ;SETUP TEST DATA
      INC      R4           ;POINT TO ODD BYTE
      CLRB     (R4)          ;*TEST INSTRUCTION
      BEQ      1#           ;BRANCH IF GOOD
                          ;CLEAR ODD BYTE FAILED

1# :   ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    61       ;UNIQUE ERROR NUMBER
      .WORD    CPUERR   ;ADDRESS OF ERROR MESSAGE

      DEC      R4           ;POINT TO EVEN BYTE
      INC      (R4)        ;LOC 0=1 0
      INC      R4           ;POINT TO ODD BYTE
      COMB     (R4)        ;*TEST INSTRUCTION
      INCB     (R4)        ;LOC 0=-1 0
      BPL      2#           ;BRANCH IF ERROR
      BEQ      2#
      INCB     (R4)
      BEQ      3#           ;BRANCH IF GOOD

```



```

1311
1312 003272
1313 003272 104000
1314 003274 000062
1315 003276 001127
1316 003300
1317
1318
1319 003300
1320
1321
1322
1323 003300
1324 003300 005267 175500
1325 003304 005004
1326 003306 105104
1327 003310 005204
1328 003312 005014
1329 003314 005114
1330 003316 005024
1331 003320 001403
1332
1333 003322 104000
1334 003324 000063
1335 003326 001127
1336 003330 005304
1337 003332 005304
1338 003334 005124
1339 003336 100004
1340 003340 005304
1341 003342 005304
1342 003344 005224
1343 003346 001403
1344
1345 003350
1346 003350 104000
1347 003352 000064
1348 003354 001127
1349 003356
1350
1351
1352 003356
1353
1354
1355
1356 003356
1357 003356 005267 175422
1358 003362 005004
1359 003364 105104
1360 003366 005204
1361 003370 005014
1362 003372 005114
1363 003374 105024
1364 003376 001403
1365
1366 003400 104000

```

```

;MODE 1, ODD BYTE FAILED
2$: ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 62 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
3$:
;
;MSPF:
;*****
;+TEST 24 TEST SINGLE OP - MODE 2 - CLR, COM, INC
;*****
TST24:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4
COMB R4
INC R4 ;R4=400
CLR (R4) ;400=0
COM (R4) ;400=-1
CLR (R4)+ ;+TEST INSTRUCTION
BEQ 1$ ;BRANCH IF GOOD
;MODE 2 CLEAR FAILED
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 63 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1$: DEC R4 ;R4=400
DEC R4 ;+TEST INSTRUCTION
COM (R4)+ ;BRANCH IF FAILURE
BPL 2$
DEC R4
DEC R4 ;R4=400
INC (R4)+ ;+TEST INSTRUCTION
BEQ 3$ ;BRANCH IF GOOD
;MODE 2 FAILURE
2$: ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 64 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
3$:
;
;MSPG:
;*****
;+TEST 25 TEST CLRB, COMB, DECB, MODE 2 - EVEN BYTE
;*****
TST25:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4
COMB R4
INC R4 ;R4=400
CLR (R4)
COM (R4) ;400=-1
CLRB (R4)+ ;+TEST INSTRUCTION
BEQ 1$ ;BRANCH IF GOOD
;MODE 2 EVEN BYTE FAILED
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR

```

```

1367 003402 000065          .WORD 65          ;UNIQUE ERROR NUMBER
1368 003404 001127          .WORD CPUERR      ;ADDRESS OF ERROR MESSAGE
1369 003406 005304          1$: DEC R4
1370 003410 105324          DECB (R4)+       ;*TEST INSTRUCTION
1371 003412 100003          BPL 2$          ;BRANCH IF BAD
1372 003414 005304          DEC R4          ;POINT TO EVEN BYTE
1373 003416 105124          COMB (R4)+      ;*TEST INSTRUCTION
1374 003420 001403          BEQ 3$          ;BRANCH IF GOOD
1375                                     ;MODE 2, EVEN BYTE FAILED
1376 003422
1377 003422 104000          2$: ERROR        ;ALL ERRORS TO TRAP TO EMT VECTOR
1378 003424 000066          .WORD 66          ;UNIQUE ERROR NUMBER
1379 003426 001127          .WORD CPUERR      ;ADDRESS OF ERROR MESSAGE
1380 003430
1381
1382
1383 003430          ;
1384                                     ;MSPH:
1385                                     ;*****
1386                                     ;*TEST 26 TEST CLR, COMB, INCB MODE 2 - ODD BYTE
1387                                     ;*****
1388 003430 005267 175350          TST26: INC $TESTN      ;INCREMENT TEST NUMBER
1389 003434 005004          CLR R4
1390 003436 105104          COMB R4
1391 003440 005204          INC R4          ;R4=400
1392 003442 005014          CLR (R4)
1393 003444 005114          COM (R4)       ;400=-1 -1
1394 003446 005214          INC (R4)       ;POINT TO ODD BYTE
1395 003450 105024          CLR (R4)+      ;*TEST INSTRUCTION
1396 003452 001403          BEQ 1$          ;BRANCH IF GOOD
1397                                     ;MODE 2, ODD BYTE FAILED
1398 003454 104000          ERROR        ;ALL ERRORS TO TRAP TO EMT VECTOR
1399 003456 000067          .WORD 67          ;UNIQUE ERROR NUMBER
1400 003460 001127          .WORD CPUERR      ;ADDRESS OF ERROR MESSAGE
1401 003462 005304          1$: DEC R4
1402 003464 005304          DEC R4
1403 003466 105224          INCB (R4)+     ;400=1 0
1404 003470 105124          COMB (R4)+     ;*TEST INSTRUCTION
1405 003472 100003          BPL 2$          ;BRANCH IF MODE 2 FAILED
1406 003474 005304          DEC R4          ;POINT TO ODD BYTE
1407 003476 105224          INCB (R4)+
1408 003500 001403          BEQ 3$          ;BRANCH IF GOOD
1409                                     ;MODE 2, ODD BYTE FAILED
1410 003502
1411 003502 104000          2$: ERROR        ;ALL ERRORS TO TRAP TO EMT VECTOR
1412 003504 000070          .WORD 70          ;UNIQUE ERROR NUMBER
1413 003506 001127          .WORD CPUERR      ;ADDRESS OF ERROR MESSAGE
1414 003510
1415
1416
1417 003510          ;
1418                                     ;MSPI:
1419                                     ;*****
1420                                     ;*TEST 27 TEST CLR, COM, INC - MODE 3
1421                                     ;*****
1422 003510 005267 175270          TST27: INC $TESTN      ;INCREMENT TEST NUMBER

```



```

1423 003514 005004          CLR      R4          ;
1424 003516 005014          CLR      (R4)        ;0=0
1425 003520 105114          COMB     (R4)        ;
1426 003522 005214          INC      (R4)        ;0=400
1427 003524 005034          CLR      @R4)+      ;*TEST INSTRUCTION
1428 003526 001403          BEQ     1$          ;BRANCH IF GOOD
1429                                ;MODE 3 FAILED, 400 SHOULD=0
1430 003530 104000          ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
1431 003532 000071          .WORD   71          ;UNIQUE ERROR NUMBER
1432 003534 001127          .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
1433 003536 005304          1$: DEC      R4
1434 003540 005304          DEC      R4          ;R4=0
1435 003542 005134          COM     @R4)+      ;*TEST INSTRUCTION
1436 003544 100004          BPL     2$          ;BRANCH IF BAD
1437 003546 005304          DEC      R4
1438 003550 005304          DEC      R4          ;REPOSITION POINTER
1439 003552 005234          INC     @R4)+      ;*TEST INSTRUCTION
1440 003554 001403          BEQ     3$          ;BRANCH IF GOOD
1441                                ;MODE 3 FAILED
1442 003556                                2$:
1443 003556 104000          ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
1444 003560 000072          .WORD   72          ;UNIQUE ERROR NUMBER
1445 003562 001127          .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
1446 003564                                3$:
1447                                ;
1448                                ;MSPJ:
1449 003564                                ;*****
1450                                ;*TEST 30      TEST CLRB, COMB, INCB - MODE 3, EVEN/ODD BYTE
1451                                ;*****
1452                                TST30:
1453 003564                                INC     @TESTN      ;INCREMENT TEST NUMBER
1454 003564 005267 175214          CLR     R4          ;R4=0
1455 003570 005004          CLR     R1
1456 003572 005001          COMB    R1
1457 003574 105101          INC     R1          ;R1=400
1458 003576 005201          CLR     (R1)
1459 003600 005011          COM     (R1)+      ;400=-1
1460 003602 005121          CLR     (R1)
1461 003604 005011          COMB    (R1)
1462 003606 105111          CLR     (R4)
1463 003610 005014          COMB    (R4)
1464 003612 105114          INC     (R4)
1465 003614 005214          CLR     @R4)+      ;
1466 003616 105034          BEQ     1$          ;0=400
1467 003620 001403          ERROR                                ;*TEST INSTRUCTION 400=377 000
1468                                ;BRANCH IF MODE 3 EVEN BYTE CLEARED
1469 003622 104000          ERROR                                ;TEST INSTRUCTION FAILED
1470 003624 000073          .WORD   73          ;ALL ERRORS TO TRAP TO EMT VECTOR
1471 003626 001127          .WORD   CPUERR      ;UNIQUE ERROR NUMBER
1472 003630 005304          1$: DEC      R4          ;ADDRESS OF ERROR MESSAGE
1473 003632 005304          DEC      R4          ;REPOSITION POINTER
1474 003634 105134          COMB    @R4)+      ;*TEST INSTRUCTION
1475 003636 005304          DEC      R4
1476 003640 005304          DEC      R4          ;REPOSITION POINTER
1477 003642 105234          INCB   @R4)+      ;*TEST INSTRUCTION
1478 003644 001403          BEQ     3$          ;BRANCH IF GOOD

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1479
1480 003646
1481 003646 104000
1482 003650 000074
1483 003652 001127
1484 003654 005304
1485 003656 005304
1486 003660 005214
1487 003662 105234
1488 003664 001004
1489 003666 005304
1490 003670 005304
1491 003672 105034
1492 003674 001403
1493
1494 003676
1495 003676 104000
1496 003700 000075
1497 003702 001127
1498 003704 005304
1499 003706 005304
1500 003710 105134
1501 003712 005304
1502 003714 005304
1503 003716 105234
1504 003720 001403
1505
1506 003722
1507 003722 104000
1508 003724 000076
1509 003726 001127
1510 003730
1511
1512
1513 003730
1514
1515
1516
1517 003730
1518 003730 005267 175050
1519 003734 005004
1520 003736 105104
1521 003740 005204
1522 003742 005014
1523 003744 005124
1524 003746 005014
1525 003750 005224
1526 003752 005044
1527 003754 001403
1528
1529 003756 104000
1530 003760 000077
1531 003762 001127
1532 003764 005344
1533 003766 005114
1534 003770 001403

2$:
ERROR
.WORD 74
.WORD CPUERR
DEC R4
DEC R4
INC (R4)
INCB @R4+
BNE 4$
DEC R4
DEC R4
CLRB @R4+
BEQ 5$

3$:
ERROR
.WORD 75
.WORD CPUERR
DEC R4
DEC R4
COMB @R4+
DEC R4
DEC R4
INCB @R4+
BEQ 7$

4$:
ERROR
.WORD 76
.WORD CPUERR

5$:
;MODE 3, EVEN BYTE FAILED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R4=401
;*TEST INSTRUCTION
;BRANCH IF 402 NEQ 0
;R4=401
;401=0
;BRANCH IF GOOD
;ODD BYTE FAILED

6$:
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R4=401
;403=377
;*TEST INSTRUCTION
;BRANCH IF GOOD
;MODE3 ODD BYTE FAILED.

7$:
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;MSPL:
;*****
;*TEST 31 TEST CLR, COM, DEC - MODE 4
;*****
TST31:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4
COMB R4
INC R4 ;R4=400
CLR (R4)
COM (R4)+ ;400=-1
CLR (R4)
INC (R4)+ ;402=1
CLR -(R4)
BEQ 1$ ;*TEST INSTRUCTION
;BRANCH IF GOOD
;MODE 4 FAILED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R4=401
;400=-1
;BRANCH IF BAD

1$:
ERROR
.WORD 77
.WORD CPUERR
DEC -(R4)
COM (R4)
BEQ 2$

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1535 003772 100404 BMI 2# ;BRANCH IF BAD
1536 003774 005204 INC R4
1537 003776 005204 INC R4 ;R4=400
1538 004000 005344 DEC -(R4) ;*TEST INSTRUCTION
1539 004002 001403 BEQ 3# ;BRANCH IF GOOD
1540 ;MODE 4 FAILED
1541 004004 2#:
1542 004004 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1543 004006 000100 .WORD 100 ;UNIQUE ERROR NUMBER
1544 004010 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1545 004012 3#:
1546
1547
1548 004012 ;
1549 ;MSPM:
1550 ;*****
1551 ;*TEST 32 TEST COMB, INCB, CLRB - MODE 4, ODD BYTE
1552 ;*****
1553 004012 005267 174766 TST32: INC #TESTN ;INCREMENT TEST NUMBER
1554 004016 005004 CLR R4
1555 004020 105104 COMB R4 ;
1556 004022 005204 INC R4 ;R4=400
1557 004024 005044 CLR -(R4) ;376=0
1558 004026 105114 COMB (R4)
1559 004030 005224 INC (R4)+ ;376=001 000
1560 004032 005014 CLR (R4)
1561 004034 005124 COM (R4)+ ;400=1
1562 004036 005204 INC R4 ;R4=403
1563 004040 105044 CLRB -(R4) ; TEST INST. CLEAR ODD BYTE (401)
1564 004042 001403 BEQ 2# ;BRANCH IF GOOD
1565 ;MODE 4 BYTE FAILED
1566 004044 1#:
1567 004044 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1568 004046 000101 .WORD 101 ;UNIQUE ERROR NUMBER
1569 004050 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1570 004052 005204 2#: INC R4
1571 004054 005204 INC R4 ;R4=403
1572 004056 105144 COMB -(R4) ; TEST INST. 401-377
1573 004060 005304 DEC R4
1574 004062 005304 DEC R4
1575 004064 105244 INCB -(R4) ; TEST INST. 401=0
1576 004066 001403 BEQ 4# ;BRANCH IF GOOD
1577 ;MODE 4 ODD BYTE FAILED
1578 004070 3#:
1579 004070 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1580 004072 000102 .WORD 102 ;UNIQUE ERROR NUMBER
1581 004074 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1582 004076 105344 4#: DECB -(R4) ;*TEST INST.
1583 004100 001403 BEQ 6# ;BRANCH IF GOOD
1584 ;MODE 4 DECREMENT ODD BYTE FAILED
1585 004102 5#:
1586 004102 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1587 004104 000103 .WORD 103 ;UNIQUE ERROR NUMBER
1588 004106 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1589 004110 6#:
1590

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1591
 1592 004110
 1593
 1594
 1595
 1596 004110
 1597 004110 005267 174670
 1598 004114 005004
 1599 004116 005014
 1600 004120 105114
 1601 004122 005224
 1602 004124 005054
 1603 004126 001403
 1604
 1605 004130 104000
 1606 004132 000104
 1607 004134 001127
 1608 004136 005204
 1609 004140 005204
 1610 004142 005154
 1611 004144 001407
 1612 004146 005204
 1613 004150 005204
 1614 004152 005354
 1615 004154 001403
 1616 004156 005224
 1617 004160 105254
 1618 004162 001403
 1619
 1620 004164
 1621 004164 104000
 1622 004166 000105
 1623 004170 001127
 1624 004172
 1625
 1626
 1627 004172
 1628
 1629
 1630
 1631 004172
 1632 004172 005267 174606
 1633 004176 005004
 1634 004200 105104
 1635 004202 005204
 1636 004204 005001
 1637 004206 105101
 1638 004210 005301
 1639 004212 005002
 1640 004214 005012
 1641 004216 005014
 1642 004220 005114
 1643 004222 005011
 1644 004224 005454
 1645 004226 001403
 1646

```

; MSPN:
;*****
; *TEST 33      TEST CLR, COM, INC - MODE 5
;*****
TST33:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      CLR      R4
      CLR      (R4)
      COMB     (R4)
      INC      (R4)+          ;0=400
      CLR      @-(R4)        ;*TEST INST. 400=0
      BEQ      1$            ;BRANCH IF GOOD
                               ;MODE 5 FAILED
                               ;ALL ERRORS TO TRAP TO EMT VECTOR
                               ;UNIQUE ERROR NUMBER
                               ;ADDRESS OF ERROR MESSAGE
1$:
      INC      R4
      COM      @-(R4)        ;RESET POINTER TO 0
      BEQ      2$            ;*TEST INST. 376=1
                               ;BRANCH IF BAD
      INC      R4
      INC      R4
      DEC      @-(R4)        ;REPOSITION POINTER
      BEQ      2$            ;*TEST INST. 376=0
                               ;BRANCH IF BAD
      INC      (R4)+
      INCB     @-(R4)        ;0=401 R4=2
      BEQ      3$            ;*TEST INST.,400= 0 376
                               ;BRANCH IF GOOD
                               ;MODE 5 FAILED
2$:
      ERROR    105           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR       ;UNIQUE ERROR NUMBER
      .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
3$:
; MSPO:
;*****
; *TEST 34      TEST NEG MODE 5
;*****
TST34:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      CLR      R4
      COMB     R4
      INC      R4            ;R4=400
      CLR      R1
      COMB     R1
      DEC      R1            ;R1=376
      CLR      R2            ;R2=0
      CLR      (R2)         ;0=0
      CLR      (R4)
      COM      (R4)
      CLR      (R1)
      NEG      @-(R4)
      BEQ      2$            ;400=-1
                               ;376=0
                               ;0=0
                               ;BRANCH IF GOOD
                               ;NEG FAILED

```


K3

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1647 004230
1648 004230 104000
1649 004232 000106
1650 004234 001127
1651 004236 005334
1652 004240 005454
1653 004242 001403
1654 004244 102402
1655 004246 100401
1656 004250 103403
1657
1658 004252
1659 004252 104000
1660 004254 000107
1661 004256 001127
1662 004260 005334
1663 004262 001403
1664
1665 004264
1666 004264 104000
1667 004266 000110
1668 004270 001127
1669 004272 105212
1670 004274 005454
1671 004276 001403
1672 004300 102402
1673 004302 103001
1674 004304 100403
1675
1676 004306
1677 004306 104000
1678 004310 000111
1679 004312 001127
1680 004314 105212
1681 004316 001403
1682 004320
1683 004320 104000
1684 004322 000112
1685 004324 001127
1686 004326
1687
1688
1689
1690 004326
1691
1692
1693
1694 004326
1695 004326 005267 174452
1696 004332 005004
1697 004334 005204
1698 004336 005204
1699 004340 005001
1700 004342 105101
1701 004344 005201
1702 004346 005011

1$:
ERROR
.WORD 106
.WORD CPUERR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
2$:
DEC 8(R4)+
NEG 8-(R4)
BEQ 3$
BVS 3$
BMI 3$
BCS 4$
;0=-1
;0=1
;BRANCH IF BAD
;BRANCH IF BAD
;BRANCH IF BAD
;BRANCH IF GOOD
;NEG FAILED
3$:
ERROR
.WORD 107
.WORD CPUERR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
4$:
DEC 8(R4)+
BEQ 6$
; TEST RESULT OF NEGATE
;BRANCH IF GOOD
;RESULT OF NEGATE BAD
5$:
ERROR
.WORD 110
.WORD CPUERR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
6$:
INCB (R2)
NEG 8-(R4)
BEQ 7$
BVS 7$
BCC 7$
BMI 8$
;0=1
;0=-1
;
;BRANCH IF GOOD
;BAD NEGATE
7$:
ERROR
.WORD 111
.WORD CPUERR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
8$:
INCB (R2)
BEQ 10$
;0=0
;BRANCH IF GOOD
9$:
ERROR
.WORD 112
.WORD CPUERR
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
10$:
;
;
MSPP:
;*****
;*TEST 35 TEST CLR, COM, INC - MODE 6
;*****
TST35:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4
INC R4
INC R4 ;R4=2
CLR R1
COMB R1
INC R1 ;R1=400
CLR (R1)

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1703 004350 005121 COM (R1)+ ;400=-1
1704 004352 005011 CLR (R1) ;R1=402
1705 004354 005211 INC (R1) ;402=1
1706 004356 005002 CLR R2 ;R2=0
1707 004360 005012 CLR (R2) ;0=0
1708 004362 005064 000376 CLR 376(R4) ;400=0
1709 004366 001403 BEQ 2# ;BRANCH IF GOOD
1710 004370 1#:
1711 004370 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1712 004372 000113 .WORD 113 ;UNIQUE ERROR NUMBER
1713 004374 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1714 004376 005364 000376 2#: DEC 376(R4) ;400=-1
1715 004402 005164 000400 COM 400(R4) ;402=-1
1716 004406 001405 BEQ 3# ;BRANCH IF BAD
1717 004410 005264 000400 INC 400(R4) ;402=-2
1718 004414 005264 000400 INC 400(R4)
1719 004420 001403 BEQ 4# ;BRANCH IF GOOD
1720 ;MODE 6 FAILED
1721 004422 3#:
1722 004422 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1723 004424 000114 .WORD 114 ;UNIQUE ERROR NUMBER
1724 004426 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1725 004430 005261 177776 4#: INC -2(R1) ;400=0
1726 004434 001403 BEQ 6# ;BRANCH IF GOOD
1727 ;ERROR! INC MODE 6 FAILED
1728 004436 5#:
1729 004436 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
1730 004440 000115 .WORD 115 ;UNIQUE ERROR NUMBER
1731 004442 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
1732 004444 6#:
1733 ;
1734 ;
1735 ;
1736 ;
1737 004444 MSPQ:
1738 ;*****
1739 ;*TEST 36 TEST NEG MODE 6
1740 ;*****
1741 J04444 TST36:
1742 004444 005267 174334 INC #TESTN ;INCREMENT TEST NUMBER
1743 004450 005001 CLR R1 ;R1=0
1744 004452 005004 CLR R4
1745 004454 105104 COMB R4
1746 004456 005204 INC R4 ;R4=400
1747 004460 005014 CLR (R4) ;
1748 004462 005114 COM (R4) ;400=-1
1749 004464 005044 CLR -(R4) ;376=0
1750 004466 005044 CLR -(R4) ;
1751 004470 005224 INC (R4)+ ;374=1 R4=376
1752 004472 005464 000002 NEG 2(R4) ;400=1
1753 004476 001403 BEQ 1# ;NEGATE FAILED
1754 004500 102402 BVS 1#
1755 004502 100401 BMI 1#
1756 004504 103403 BCS 2# ;BRANCH IF GOOD
1757 ;NEGATE FAILED
1758 004506 1#:

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1759 004506 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
1760 004510 000116          .WORD          116          ; UNIQUE ERROR NUMBER
1761 004512 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
1762 004514 005364 000002   2$: DEC          2(R4)      ; TEST RESULT OF NEGATE
1763 004520 001403          BEQ           4$          ; BRANCH IF GOOD
1764                                     ; RESULT OF NEGATE FAILED
1765 004522                                     3$:
1766 004522 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
1767 004524 000117          .WORD          117          ; UNIQUE ERROR NUMBER
1768 004526 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
1769 004530 005464 000000   4$: NEG          0(R4)      ; *0=0
1770 004534 001403          BEQ           5$          ; BRANCH IF GOOD
1771                                     ; NEGATE FAILED
1772 004536 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
1773 004540 000120          .WORD          120          ; UNIQUE ERROR NUMBER
1774 004542 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
1775 004544 105461 000374   5$: NEGB        374(R1)    ; 374=0 377
1776 004550 102403          BVS          6$          ;
1777 004552 001402          BEQ          6$          ;
1778 004554 100001          BPL          6$          ;
1779 004556 103403          BCS          7$          ; BRANCH IF GOOD
1780                                     ; NEGATE FAILED
1781 004560                                     6$:
1782 004560 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
1783 004562 000121          .WORD          121          ; UNIQUE ERROR NUMBER
1784 004564 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
1785 004566 105261 000374   7$: INCB        374(R1)    ; 374=0
1786 004572 001403          BEQ          9$          ; BRANCH IF GOOD
1787                                     ; NEGATE FAILED
1788 004574                                     8$:
1789 004574 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
1790 004576 000122          .WORD          122          ; UNIQUE ERROR NUMBER
1791 004600 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
1792 004602                                     9$:
1793                                     ;
1794                                     ;
1795 004602                                     ; MSPR:
1796                                     ; *****
1797                                     ; *TEST 37      TEST CLR, COM, INC - MODE 7
1798                                     ; *****
1799 004602                                     TST37:
1800 004602 005267 174176   INC          $TESTN      ; INCREMENT TEST NUMBER
1801 004606 005001          CLR          R1          ; R1=0
1802 004610 005004          CLR          R4          ;
1803 004612 105104          COMB        R4          ;
1804 004614 005204          INC          R4          ; R4=400
1805 004616 005011          CLR          (R1)
1806 004620 105111          COMB        (R1)
1807 004622 005211          INC          (R1)
1808 004624 005211          INC          (R1)
1809 004626 005211          INC          (R1)
1810 004630 005014          CLR          (R4)      ; ;0=402
1811 004632 005064 000002   CLR          2(R4)      ; 400=0
1812 004636 005164 000002   COM          2(R4)      ; 402=-1
1813 004642 005074 177400   CLR          8-400(R4)  ; 402=0
1814 004646 001403          BEQ          2$          ; BRANCH IF GOOD

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```

1815 004650          1$:
1816 004650 104000      ERROR
1817 004652 000123      .WORD 123
1818 004654 001127      .WORD CPUERR
1819
1820 004656 005171 000000 2$: COM 80(R1)
1821 004662 100403      BMI 4$
1822 004664          3$:
1823 004664 104000      ERROR
1824 004666 000124      .WORD 124
1825 004670 001127      .WORD CPUERR
1826
1827 004672 005104          4$: COM R4
1828 004674 005274 000401      INC 8401(R4)
1829 004700 001403      BEQ 6$
1830
1831 004702 104000          5$: ERROR
1832 004704 000125      .WORD 125
1833 004706 001127      .WORD CPUERR
1834
1835 004710          6$:
1836
1837
1838 004710
1839
1840
1841
1842 004710
1843 004710 005267 174070      ; MSPS:
1844 004714 005004          ; *****
1845 004716 005014          ; *TEST 40 TEST NEG MODE 7
1846 004720 005002          ; *****
1847 004722 105102          TST40:
1848 004724 005202          INC $TESTN
1849 004726 005012          CLR R4
1850 004730 005472 177400      CLR (R4)
1851 004734 103401          CLR R2
1852 004736 001403          COMB R2
1853 004740          1$: INC R2
1854 004740 104000          CLR (R2)
1855 004742 000126          NEG 8-400(R2)
1856 004744 001127          BCS 1$
1857
1858 004746 005314          BEQ 2$
1859 004750 005474 000400      BCS 2$
1860 004754 001403          2$: DEC (R4)
1861 004756 102402          NEG 8+400(R4)
1862 004760 100401          BEQ 3$
1863 004762 103403          BVS 3$
1864 004764          3$: BMI 3$
1865 004764 104000          BCS 4$
1866 004766 000127          4$: ERROR
1867 004770 001127      .WORD 127
1868
1869 004772          .WORD CPUERR
1870

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; INSTRUCTION FAILED
; 402=-1
; BRANCH IF GOOD
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; 402=0
; BRANCH IF GOOD
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; MODE 7 FAILED

```

```

; MSPS:
; *****
; *TEST 40 TEST NEG MODE 7
; *****
TST40:

```

```

; INCREMENT TEST NUMBER
; 0=0
;
; R2=400
; 400=0
; NEG OF 0=0
; *****
; BRANCH IF GOOD
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
;
; 0=-1
; 0=1
; BRANCH IF ERROR
;
; BRANCH IF GOOD
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; NEGATE MODE 7 FAILED

```



```

1871
1872 004772
1873
1874
1875
1876 004772
1877 004772 005267 174006
1878 004776 005004
1879 005000 105104
1880 005002 005204
1881 005004 005027
1882 005006 177777
1883 005010 001403
1884 005012
1885 005012 104000
1886 005014 000130
1887 005016 001127
1888 005020
1889
1890
1891
1892 005020
1893
1894
1895
1896 005020
1897 005020 005267 173760
1898 005024 005004
1899 005026 000277
1900 005030 000244
1901 005032 005704
1902 005034 103403
1903 005036 102402
1904 005040 100401
1905 005042 001403
1906 005044
1907 005044 104000
1908 005046 000131
1909 005050 001127
1910
1911 005052 005304
1912 005054 000277
1913 005056 000250
1914 005060 005704
1915 005062 103403
1916 005064 102402
1917 005066 001401
1918 005070 100403
1919 005072
1920 005072 104000
1921 005074 000132
1922 005076 001127
1923
1924 005100
1925
1926

;
MSPT:
;*****
;+TEST 41 TEST SINGLE OPERAND MODE 2 REG 7
;*****
TST41:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4
COMB R4
INC R4 ;R4=400
CLR (R7)+ ;CLEAR NEXT LOCATION
10: .WORD -1 ;SETUP INITIAL DATA
BEQ 30 ;BRANCH IF GOOD
20: ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 130 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
30:
;
MSPU:
;*****
;+TEST 42 TEST TST MODE 0
;*****
TST42:
INC $TESTN ;INCREMENT TEST NUMBER
CLR R4 ;R4=0
SCC ;CONDITION CODES =1111
CLZ ;CC=1011
TST R4 ;+TEST INSTRUCTION
BCS 10
BVS 10
BMI 10 ;BRANCH IF ERROR
BEQ 20 ;BRANCH IF GOOD
10: ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 131 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
20: ;TST MODE 0 FAILED
DEC R4 ;R4=-1
SCC
CLN ;CC=0111
TST R4 ;+TEST INSTRUCTION MODE 0
BCS 30 ;BRANCH IF ERROR
BVS 30
BEQ 30
BMI 40 ;BRANCH IF GOOD
30: ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 132 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
40: ;TST FAILED
;

```



```

1983 005216 103401          BCS      3#
1984 005220 100003          BPL      4#          ;BRANCH IF GOOD
1985 005222                3#:
1986 005222 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
1987 005224 000136          .WORD    136          ;UNIQUE ERROR NUMBER
1988 005226 001127          .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
1989
1990 005230                4#:          ;TST FAILED MODE 1
1991
1992
1993 005230                ;
1994                ;MSPX:
1995                ;*****
1996                ;*TEST 45      TEST TST MODE 1 BYTE
1997                ;*****
1998 005230 005267 173550    TST45:
1999 005234 005004          INC      $TESTN       ;INCREMENT TEST NUMBER
2000 005236 005014          CLR      R4           ;R4=0
2001 005240 105114          CLR      (R4)
2002 005242 005214          COMB    (R4)
2003 005244 000277          INC      (R4)       ;0=001 000
2004 005246 000244          SCC
2005 005250 105714          CLZ
2006 005252 103403          TSTB    (R4)       ;CC=1011
2007 005254 102402          BCS     1#          ;*TEST INTRUCTION
2008 005256 100401          BVS     1#          ;BRANCH IF ERROR
2009 005260 001403          BMI     1#
2010 005262                BEQ     2#          ;BRANCH IF GOOD
2011 005262 104000          1#:          ERROR
2012 005264 000137          .WORD    137          ;ALL ERRORS TO TRAP TO EMT VECTOR
2013 005266 001127          .WORD    CPUERR       ;UNIQUE ERROR NUMBER
2014
2015 005270 005204                .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2016 005272 000277          2#:          INC      R4           ;R4=1
2017 005274 105714          SCC
2018 005276 001403          TSTB    (R4)       ; TEST INSTRUCTION
2019 005300 100402          BEQ     3#          ;BRANCH IF ERROR
2020 005302 102401          BMI     3#
2021 005304 103003          BVS     3#
2022 005306                BCC     4#          ;BRANCH IF GOOD
2023 005306 104000          3#:          ERROR
2024 005310 000140          .WORD    140          ;ALL ERRORS TO TRAP TO EMT VECTOR
2025 005312 001127          .WORD    CPUERR       ;UNIQUE ERROR NUMBER
2026
2027 005314                .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2028
2029
2030 005314                ;
2031                ;MSPY:
2032                ;*****
2033                ;*TEST 46      TEST TST MODE 2
2034                ;*****
2035 005314 005267 173464    TST46:
2036 005320 005004          INC      $TESTN       ;INCREMENT TEST NUMBER
2037 005322 005024          CLR      R4           ;
2038 005324 005014          CLR      (R4)       ;0=0
                CLR      (R4)

```

```

2039 005326 005114 COM (R4) ;2=-1
2040 005330 005004 CLR R4 ;R4=0
2041 005332 000277 SCC ;
2042 005334 000244 CLZ ;CC=1011
2043 005336 005724 TST (R4); ; TEST INSTRUCTION
2044 005340 103403 BCS 1# ;BRANCH IF ERROR
2045 005342 102402 BVS 1#
2046 005344 100401 BMI 1#
2047 005346 001403 BEQ 2# ;BRANCH IF GOOD
2048 005350 1# :
2049 005350 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
2050 005352 000141 .WORD 141 ;UNIQUE ERROR NUMBER
2051 005354 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
2052 ;MODE 2 TEST FAILED
2053 005356 005724 2# : TST (R4); ;TST LOC2
2054 005360 103403 BCS 3#
2055 005362 102402 BVS 3#
2056 005364 001401 BEQ 3#
2057 005366 100403 BMI 4#
2058 005370 3# :
2059 005370 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
2060 005372 000142 .WORD 142 ;UNIQUE ERROR NUMBER
2061 005374 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
2062 ;MODE 2 FAILED
2063 005376 4# :
2064
2065
2066 005376 ;
2067 ;MSPZ:
2068 ;*****
2069 ;*TEST 47 TEST TST MODE 2 BYTE
2070 ;*****
2071 005376 005267 173402 TST47: INC #TESTN ;INCREMENT TEST NUMBER
2072 005402 005004 CLR R4
2073 005404 005024 CLR (R4); ;
2074 005406 105144 COMB -(R4) ;0=377 000
2075 005410 005304 DEC R4 ;R4=0
2076 005412 000277 SCC ;
2077 005414 000244 CLZ ;CC=1011
2078 005416 105724 TSTB (R4); ;
2079 005420 102403 BVS 1# ;BRANCH IF ERROR
2080 005422 103402 BCS 1#
2081 005424 100401 BMI 1#
2082 005426 001403 BEQ 2# ;BRANCH IF GOOD
2083 005430 1# :
2084 005430 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
2085 005432 000143 .WORD 143 ;UNIQUE ERROR NUMBER
2086 005434 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
2087 ;MODE 2 EVEN BYTE FAILED
2088 005436 000277 2# : SCC ;CC=0111
2089 005440 000250 CLN ;
2090 005442 105724 TSTB (R4); ;
2091 005444 001403 BEQ 3# ;
2092 005446 103402 BCS 3# ;
2093 005450 102401 BVS 3# ;
2094 005452 100403 BMI 4# ;BRANCH IF GOOD

```



```

2095 005454          3#:
2096 005454 104000  ERROR
2097 005456 000144  .WORD 144
2098 005460 001127  .WORD CPUERR
2099
2100 005462          4#:
2101
2102
2103 005462          ;
2104          ;MSPAA:
2105          ;*****
2106          ;*TEST 50      TEST TST MODE 3
2107          ;*****
2108 005462 005267 173316  TST50:
2109 005466 005004          INC      $TESTN          ;INCREMENT TEST NUMBER
2110 005470 005014          CLR      R4
2111 005472 105114          CLR      (R4)
2112 005474 005214          COMB    (R4)
2113 005476 005034          INC      (R4)          ;0=400
2114 005500 005004          CLR      @R4)         ;400=0
2115 005502 000277          CLR      R4           ;R4=0
2116 005504 000244          SCC
2117 005506 005734          CLZ          ;CC=1011
2118 005510 103403          TST      @R4)         ; TEST MODE 3
2119 005512 102402          BCS      1#           ;BRANCH IF ERROR
2120 005514 100401          BVS      1#
2121 005516 001403          BMI      1#
2122 005520          1#:          BEQ      2#           ;BRANCH IF GOOD
2123 005520 104000  ERROR
2124 005522 000145  .WORD 145
2125 005524 001127  .WORD CPUERR
2126
2127 005526 005304          2#:          DEC      R4
2128 005530 005304          DEC      R4           ;R4=0
2129 005532 005334          DEC      @R4)         ;400=-1
2130 005534 005004          CLR      R4
2131 005536 000277          SCC
2132 005540 000250          CLN
2133 005542 005734          TST      @R4)         ;CC=0111
2134 005544 103403          BCS      3#           ; TEST INSTRUCTION
2135 005546 001402          BEQ      3#           ;BRANCH IF ERROR
2136 005550 102401          BVS      3#
2137 005552 100403          BMI      4#           ;BRANCH IF GOOD
2138
2139 005554          3#:          ;ERROR MODE 3
2140 005554 104000  ERROR
2141 005556 000146  .WORD 146
2142 005560 001127  .WORD CPUERR
2143
2144          4#:
2145
2146 005562          ;
2147          ;MSPBB:
2148          ;*****
2149          ;*TEST 51      TEST TST MODE 3 AUTO-INC
2150 005562          ;*****
                TST51:

```

```

2151 005562 005267 173216      INC      $TESTN      ;INCREMENT TEST NUMBER
2152 005566 005004              CLR      R4
2153 005570 005014              CLR      (R4)      ;0=0
2154 005572 105114              COMB     (R4)
2155 005574 005214              INC      (R4)      ;0=400
2156 005576 005001              CLR      R1
2157 005600 105101              COMB     R1
2158 005602 005201              INC      R1      ;R1=400
2159 005604 005011              CLR      (R1)     ;400=0
2160 005606 000277              SCC
2161 005610 005734              TST     @R4)+     ;400=0
2162 005612 103403              BCS     1#        ;ERROR IF CARRY
2163 005614 102402              BVS     1#        ;ERROR IF OVERFLOW
2164 005616 100401              BMI     1#        ;ERROR IF MINUS
2165 005620 001403              BEQ     2#        ;ERROR IF NOT EQUAL
2166
2167 005622                      1#:
2168 005622 104000              ERROR
2169 005624 000147              .WORD   147      ;ALL ERRORS TO TRAP TO EMT VECTOR
2170 005626 001127              .WORD   CPUERR  ;UNIQUE ERROR NUMBER
2171 005630 005304              DEC      R4      ;ADDRESS OF ERROR MESSAGE
2172 005632 005304              DEC      R4
2173 005634 005704              TST     R4
2174 005636 001403              BEQ     4#        ;SEE IF AUTO-INC WORKED
2175
2176 005640                      3#:
2177 005640 104000              ERROR
2178 005642 000150              .WORD   150      ;ALL ERRORS TO TRAP TO EMT VECTOR
2179 005644 001127              .WORD   CPUERR  ;UNIQUE ERROR NUMBER
2180 005646                      4#:
2181
2182
2183 005646                      ;
2184
2185
2186
2187 005646                      ;*****
2188 005646 005267 173132      TST52:  INC      $TESTN      ;INCREMENT TEST NUMBER
2189 005652 005004              CLR      R4
2190 005654 005014              CLR      (R4)
2191 005656 105114              COMB     (R4)
2192 005660 005214              INC      (R4)
2193 005662 005214              INC      (R4)      ;0=401
2194 005664 005001              CLR      R1
2195 005666 105101              COMB     R1
2196 005670 005201              INC      R1      ;R1=400
2197 005672 005011              CLR      (R1)
2198 005674 005111              COM      (R1)
2199 005676 105011              CLRB    (R1)
2200 005700 105734              TSTB    @R4)+     ;400=377 000
2201 005702 001403              BEQ     1#        ;** TEST INSTRUCTION
2202 005704 103402              BCS     1#        ;ERROR IF EQUAL
2203 005706 102401              BVS     1#        ;ERROR IR OVERFLOW
2204 005710 100403              BMI     2#        ;BRANCH IF MINUS
2205
2206 005712                      1#:

```



```

2207 005712 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2208 005714 000151        .WORD      151          ;UNIQUE ERROR NUMBER
2209 005716 001127        .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
2210 005720 005304        2$: DEC      R4
2211 005722 005304        DEC      R4
2212 005724 001403        BEQ      4$            ;BRANCH IF AUTO-INC WORKED
2213                                     ;AUTO-INC FAILED
2214 005726        3$:
2215 005726 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2216 005730 000152        .WORD      152          ;UNIQUE ERROR NUMBER
2217 005732 001127        .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
2218 005734        4$:
2219
2220
2221 005734        ;
2222        MST4:
2223        ;*****
2224        ;*TEST 53          TEST TST MODE 4
2225        ;*****
2226 005734 005267 173044    TST53:
2227 005740 005004          INC      $TESTN        ;INCREMENT TEST NUMBER
2228 005742 005014          CLR      R4
2229 005744 005204          CLR      (R4)         ;0=0
2230 005746 005204          INC      R4
2231 005750 000277          INC      R4           ;R4=2
2232 005752 000244          SCC
2233 005754 005744          CLZ
2234 005756 103403          TST      -(R4)       ;CC=1011
2235 005760 102402          BCS      1$          ;**TEST INTRUCTION
2236 005762 100401          BVS      1$          ;ERROR IF CARRY
2237 005764 001403          BMI      1$          ;ERROR IF OVERFLOW
2238                                     ;ERROR IF MINUS
2239 005766        1$: BEQ      2$          ;BRANCH IF GOOD
2240 005766 104000          ;ERROR! CC WRONG
2241 005770 000153        ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2242 005772 001127        .WORD      153          ;UNIQUE ERROR NUMBER
2243 005774 005704        .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
2244 005776 001403        2$: TST      R4
2245                                     ;INSURE CORRECT AUTO-DEC
2246 006000        3$: BEQ      4$          ;BRANCH IF GOOD AUTO-DEC
2247 006000 104000          ;BAD AUTO-DEC
2248 006002 000154        ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2249 006004 001127        .WORD      154          ;UNIQUE ERROR NUMBER
2250 006006        4$: .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
2251
2252
2253 006006        ;
2254        MST4B:
2255        ;*****
2256        ;*TEST 54          TEST TST MODE 4 BYTE
2257        ;*****
2258 006006 005267 172772    TST54:
2259 006012 005004          INC      $TESTN        ;INCREMENT TEST NUMBER
2260 006014 005014          CLR      R4
2261 006016 005114          CLR      (R4)
2262 006020 105114          COM      (R4)
                                     ;0=377 000
                                     COMB     (R4)

```

```

2263 006022 000277          SCC
2264 006024 005204          INC      R4
2265 006026 005204          INC      R4
2266 006030 105744          TSTB    -(R4)
2267 006032 001403          BEQ     1#
2268 006034 103402          BCS     1#
2269 006036 102401          BVS     1#
2270 006040 100403          BMI     2#
2271
2272 006042          1#:
2273 006042 104000          ERROR
2274 006044 000155          .WORD  155
2275 006046 001127          .WORD  CPUERR
2276 006050 105744          2#:  TSTB    -(R4)
2277 006052 001403          BEQ     4#
2278
2279 006054          3#:
2280 006054 104000          ERROR
2281 006056 000156          .WORD  156
2282 006060 001127          .WORD  CPUERR
2283 006062          4#:
2284
2285 006062          ;
2286          ;MST5:
2287          ;*****
2288          ;*TEST 55      TEST TST MODE 5
2289          ;*****
2290 006062 005267 172716    TST55:
2291 006066 005004          INC     #TESTN
2292 006070 005024          CLR     R4
2293 006072 000277          CLR     (R4)+
2294 006074 000244          SCC
2295 006076 005754          CLZ
2296 006100 103403          TST    8-(R4)
2297 006102 102402          BCS     1#
2298 006104 100401          BVS     1#
2299 006106 001403          BMI     1#
2300          BEQ     2#
2301 006110          1#:
2302 006110 104000          ERROR
2303 006112 000157          .WORD  157
2304 006114 001127          .WORD  CPUERR
2305 006116 005704          2#:  TST     R4
2306 006120 001403          BEQ     4#
2307
2308 006122          3#:
2309 006122 104000          ERROR
2310 006124 000160          .WORD  160
2311 006126 001127          .WORD  CPUERR
2312 006130          4#:
2313
2314          ;
2315 006130          ;MST58:
2316          ;*****
2317          ;*TEST 56      TEST TST MODE 5 BYTE
2318          ;*****

```

```

;R4=2
; **TEST INSTRUCTION
; ERROR IF EQUAL TO 0
; ERROR IF CARRY
; ERROR IF OVERFLOW
; BRANCH IF MINUS
; ERROR! CC SHOULD EQUAL 0100

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

; **TEST EVEN BYTE
; BRANCH IF GOOD
; ERROR! CC SHOULD EQUAL 0100 AND R4=-1

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

; INCREMENT TEST NUMBER
; 0=0, R4=2

; CC=1011
; TEST INSTRUCTION
; ERROR IF CARRY
; ERROR IF OVERFLOW
; ERROR IF MINUS
; BRANCH IF GOOD
; ERROR! CC WRONG, SHOULD = 0100

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

; BRANCH IF AUTO-DEC WORKED
; ERROR! AUTO-DEC FAILED

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

```



```

2319 006130
2320 006130 005267 172650
2321 006134 005004
2322 006136 005014
2323 006140 105114
2324 006142 005214
2325 006144 005034
2326 006146 005154
2327 006150 105134
2328 006152 105754
2329 006154 103403
2330 006156 100402
2331 006160 102401
2332 006162 001403
2333
2334 006164
2335 006164 104000
2336 006166 000161
2337 006170 001127
2338 006172 005224
2339 006174 105754
2340 006176 100403
2341
2342 006200
2343 006200 104000
2344 006202 000162
2345 006204 001127
2346 006206
2347
2348
2349 006206
2350
2351
2352
2353 006206
2354 006206 005267 172572
2355 006212 005004
2356 006214 005014
2357 006216 105104
2358 006220 005204
2359 006222 005014
2360 006224 005114
2361 006226 005764 177400
2362 006232 103403
2363 006234 102402
2364 006236 100401
2365 006240 001403
2366
2367 006242
2368 006242 104000
2369 006244 000163
2370 006246 001127
2371 006250 005004
2372 006252 005764 000400
2373 006256 001401
2374 006260 100403

TST56:
INC      $TESTN          ;INCREMENT TEST NUMBER
CLR      R4
CLR      (R4)
COMB     (R4)
INC      (R4)            ;0=400
CLR      @-(R4)+         ;400=0, R4=2
COM      @-(R4)
COMB     @-(R4)+         ;400=377 000 R4=2
TSTB    @-(R4)          ;**TEST INSTRUCTION
BCS      1#             ;ERROR IF CARRY
BMI      1#             ;ERROR IF MINUS
BVS      1#             ;ERROR IF OVERFLOW
BEQ      2#             ;BRANCH IF GOOD
                    ;ERROR! CC SHOULD = 0100

1#:
ERROR
.WORD    161            ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD    CPUERR        ;UNIQUE ERROR NUMBER
                    ;ADDRESS OF ERROR MESSAGE

2#:
INC      (R4)+         ;0=401
TSTB    @-(R4)          ;**TEST INSTRUCTION
BMI      4#             ;BRANCH IF GOOD
                    ;EVEN BYTE FAILURE

3#:
ERROR
.WORD    162            ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD    CPUERR        ;UNIQUE ERROR NUMBER
                    ;ADDRESS OF ERROR MESSAGE

4#:

;
;MST6:
;*****
;+TEST 57      TEST TST MODE 6
;*****
TST57:
INC      $TESTN          ;INCREMENT TEST NUMBER
CLR      R4
CLR      (R4)            ;0=0
COMB     R4              ;R4=400
INC      R4
CLR      (R4)
COM      (R4)            ;400=-1
TST      -400(R4)        ;**TEST LOCATION 0
BCS      1#             ;ERROR IF CARRY
BVS      1#             ;ERROR IF OVERFLOW
BMI      1#             ;ERROR IF MINUS
BEQ      2#             ;BRANCH IF ZERO
                    ;ERROR! CC ARE WRONG

1#:
ERROR
.WORD    163            ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD    CPUERR        ;UNIQUE ERROR NUMBER
                    ;ADDRESS OF ERROR MESSAGE

2#:
CLR      R4
TST      400(R4)        ;TST LOCATION 400
BEQ      3#             ;ERROR IF EQUAL
BMI      4#             ;BRANCH IF MINUS

```

```

2375                                     ;ERROR! CC ERROR
2376 006262                               3$:
2377 006262 104000                        ERROR
2378 006264 000164                        .WORD 164
2379 006266 001127                        .WORD CPUERR
2380 006270
2381
2382
2383 006270
2384
2385
2386
2387 006270
2388 006270 005267 172510
2389 006274 005004
2390 006276 005014
2391 006300 005124
2392 006302 005014
2393 006304 005002
2394 006306 005004
2395 006310 105104
2396 006312 005204
2397 006314 005014
2398 006316 005774 177402
2399 006322 103403
2400 006324 102402
2401 006326 001401
2402 006330 100403
2403
2404 006332                               1$:
2405 006332 104000                        ERROR
2406 006334 000165                        .WORD 165
2407 006336 001127                        .WORD CPUERR
2408 006340 005222                               2$:
2409 006342 005774 177402                INC (R2)+
2410 006346 100401                        TST 0-376(R4)
2411 006350 001403                        BMI 3$
2412
2413
2414 006352                               3$:
2415 006352 104000                        ERROR
2416 006354 000166                        .WORD 166
2417 006356 001127                        .WORD CPUERR
2418
2419
2420
2421 006360
2422
2423
2424
2425 006360
2426 006360 005267 172420
2427 006364 005004
2428 006366 005001
2429 006370 005101
2430 006372 010104
    
```

```

;*****
;*TEST 60 TEST TST MODE 7
;*****
TST60:
    INC    $TESTN           ;INCREMENT TEST NUMBER
    CLR    R4
    CLR    (R4)
    COM    (R4)+           ;0=-1
    CLR    (R4)           ;2=0
    CLR    R2             ;R2=0
    CLR    R4
    COMB   R4
    INC    R4             ;R4=400
    CLR    (R4)          ;400=0
    TST    0-376(R4)     ;**TEST LOCATION 0
    BCS    1$           ;ERROR IF CARRY
    BVS    1$           ;ERROR IF OVERFLOW
    BEQ    1$           ;ERROR IF ZERO
    BMI    2$           ;BRANCH IF GOOD
    ;ERROR! ERROR IN CC

    ;*****
    ;*TEST 61 TEST MOVE MODE 0
    ;*****
TST61:
    INC    $TESTN           ;INCREMENT TEST NUMBER
    CLR    R4             ;R4=0
    CLR    R1
    COM    R1             ;R1=-1
    MOV    R1,R4         ;**TEST MOVE INSTRUCTION
    
```



```

2487 006504          1#:
2488 006504 104000      ERROR
2489 006506 000172      .WORD 172
2490 006510 001127      .WORD CPUERR
2491 006512 005101      2#: COM R1
2492 006514 005201      INC R1
2493 006516 160104      SUB R1,R4
2494 006520 001403      BEQ 4#
2495
2496 006522          3#:
2497 006522 104000      ERROR
2498 006524 000173      .WORD 173
2499 006526 001127      .WORD CPUERR
2500 006530          4#:
2501
2502
2503 006530          ;
2504          ;MDM27:
2505          ;*****
2506          ;*TEST 64      TEST MOV MODE 27,00
2507          ;*****
2508 006530 005267 172250  TST64:
2509 006534 000257          INC #TESTN
2510 006536 012704 125252  CCC
2511 006542 001401          MOV #125252,R4
2512 006544 100403          BEQ 1#
2513          BMI 2#
2514 006546          1#:
2515 006546 104000      ERROR
2516 006550 000174      .WORD 174
2517 006552 001127      .WORD CPUERR
2518 006554 012701 052525  2#: MOV #052525,R1
2519 006560 100401          BMI 3#
2520 006562 001003          BNE 4#
2521
2522 006564          3#:
2523 006564 104000      ERROR
2524 006566 000175      .WORD 175
2525 006570 001127      .WORD CPUERR
2526 006572 060104      4#: ADD R1,R4
2527 006574 100403      BMI 6#
2528
2529 006576          5#:
2530 006576 104000      ERROR
2531 006600 000176      .WORD 176
2532 006602 001127      .WORD CPUERR
2533 006604 005204      6#: INC R4
2534 006606 001373      BNE 5#
2535
2536          ;
2537 006610          ;MBI00:
2538          ;*****
2539          ;*TEST 65      TEST BIC, BIS MODE 0,0
2540          ;*****
2541 006610          TST65:
2542 006610 005267 172170  INC #TESTN

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; R1=1
; GET TWO'S COMPLIMENT, R1=-1
; **TEST R4-R1 (1- 1= 0)
; BRANCH IF ZERO
; ERROR! CC SHOULD = 0100

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

```

```

; INCREMENT TEST NUMBER
; CC=0000
; **TEST MOVE
; ERROR IF = 0
; BRANCH IF MINUS
; ERROR! CC SHOULD = 1000

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; **TEST MOVE
; ERROR IF MINUS
; BRANCH IF NE 0
; ERROR! CC SHOULD = 0000

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; R1+R4=-1
; BRANCH IF MINUS
; ERROR! MOV FAILED

```

```

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; R4+1=0
; ERROR IF NOT ZERO

```

```

; INCREMENT TEST NUMBER

```



```

2543 006614 005004          CLR      R4
2544 006616 005104          COM      R4
2545 006620 012701 125252  MOV      #125252,R1
2546 006624 012702 052525  MOV      #052525,R2
2547 006630 000261          SEC
2548 006632 040104          BIC      R1,R4
2549 006634 103003          BCC      1#
2550 006636 102402          BVS      1#
2551 006640 001401          BEQ      1#
2552 006642 100003          BPL      2#
2553
2554 006644          1#:
2555 006644 104000          ERROR
2556 006646 000177          .WORD   177
2557 006650 001127          .WORD   CPUERR
2558 006652 020402          2#:  CMP      R4,R2
2559 006654 001403          BEQ      4#
2560
2561 006656          3#:
2562 006656 104000          ERROR
2563 006660 000200          .WORD   200
2564 006662 001127          .WORD   CPUERR
2565 006664 005301          4#:  DEC      R1
2566 006666 050201          BIS      R2,R1
2567 006670 100403          BMI      6#
2568
2569 006672          5#:
2570 006672 104000          ERROR
2571 006674 000201          .WORD   201
2572 006676 001127          .WORD   CPUERR
2573 006700 005201          6#:  INC      R1
2574 006702 005201          INC      R1
2575 006704 005201          INC      R1
2576 006706 001371          BNE      5#
2577
2578
2579 006710          ;
2580          ;MBC00:
2581          ;*****
2582          ;*TEST 66      TEST BIT, CMP MODE 0,0
2583          ;*****
2584 006710          TST66:
2585 006714 005267 172070  INC      #TESTN
2586 006720 012704 100000  MOV      #125252,R1
2587 006724 012702 052525  MOV      #100000,R4
2588 006730 030401          MOV      #052525,R2
2589 006732 001401          BIT      R4,R1
2590 006734 100403          BEQ      1#
2591          BMI      2#
2592
2593 006736          1#:
2594 006740 000202          ERROR
2595 006742 001127          .WORD   202
2596 006744 020401          .WORD   CPUERR
2597 006746 001402          2#:  CMP      R4,R1
2598 006750 103001          BEQ      3#
          BCC      3#

```

;R4=-1
;SETUP R1 TEST DATA
;R2=COMPLIMENT OF R1
; **TEST BIC WITH CARRY SET
;ERROR IF NO CARRY
;ERROR IF OVERFLOW
;ERROR IF 0
;BRANCH IF PLUS
;ERROR! CC SHOULD = 0001
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;COMPARE CONTENTS OF R4 AND R2
;BRANCH IF EQUAL
;ERROR! R4 AND R2 SHOULD BE EQUAL
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R1=125251
;BIS 052525 AND 125251=177775
;BRANCH IF MINUS VALUE
;ERROR! BAD BIS OPERATION
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R1=0
;ERROR IF NE 0
;INCREMENT TEST NUMBER
;R1=125252
;R4=100000
;R2=052525
; **TEST OF BIT .CC=1000
;ERROR IF EQ 0
;BRANCH IF GOOD
;ERROR! CC SHOULD = 1000
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;*TEST 100000-125252=25252
;ERROR IF EQUAL 0
;ERROR IF CARRY CLEARED

```

2599 006752 100403          BMI      40          ;BRANCH IF GOOD
2600                                ;ERROR! CC SHOULD = 0010
2601 006754          30:          ;
2602 006754 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2603 006756 000203          .WORD    203          ;UNIQUE ERROR NUMBER
2604 006760 001127          .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2605 006762 020104          40:    CMP      R1,R4          ;125252-100000 = 25252
2606 006764 001403          BEQ      50          ;ERROR IF EQUAL
2607 006766 103402          BCS      50          ;ERROR IF CARRY
2608 006770 102401          BVS      50          ;ERROR IF OVERFLOW
2609 006772 100003          BPL      60          ;BRANCH IF GOOD
2610                                ;ERROR! CC SHOULD =0001
2611 006774          50:          ;
2612 006774 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2613 006776 000204          .WORD    204          ;UNIQUE ERROR NUMBER
2614 007000 001127          .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2615 007002 005004          60:    CLR      R4          ;R4=1
2616 007004 005204          INC      R4          ;
2617 007006 000277          SCC          ;
2618 007010 030401          BIT      R4,R1       ;R4 + R1 = 2
2619 007012 001403          BEQ      80          ;BRANCH IF GOOD
2620                                ;ERROR! CC SHOULD = 0101
2621 007014          70:          ;
2622 007014 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2623 007016 000205          .WORD    205          ;UNIQUE ERROR NUMBER
2624 007020 001127          .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2625 007022          80:          ;
2626                                ;
2627                                ;
2628 007022          ;
2629                                ;
2630                                ;*****
2631                                ;*TEST 67      TEST MOV, MOVB MODE 1,1 AND SIGN EXT ON MOVB TO GPR
2632                                ;*****
2633 007022 005267 171756          TST67:  INC      $TESTN          ;INCREMENT TEST NUMBER
2634 007026 012704 000400          MOV      $400,R4          ;R4=400
2635 007032 012701 000402          MOV      $402,R1          ;R1=402
2636 007036 005014          CLR      (R4)          ;
2637 007040 005114          COM      (R4)          ;400--1
2638 007042 005011          CLR      (R1)          ;
2639 007044 105111          COMB     (R1)          ;402=000 377
2640 007046 005002          CLR      R2          ;R2=0
2641 007050 012703 000405          MOV      $405,R3          ;R3=405
2642 007054 000277          SCC          ;CC=1111
2643 007056 011412          MOV      (R4),(R2)       ;MOV 400 TO 0 ,0--1
2644 007060 001403          BEQ      10          ;ERROR IF 0
2645 007062 102402          BVS      10          ;ERROR IF OVERFLOW
2646 007064 103001          BCC      10          ;ERROR IF NO CARRY
2647 007066 100403          BMI      20          ;BRANCH IF GOOD
2648                                ;ERROR! CC SHOULD =1001
2649 007070          10:          ;
2650 007070 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2651 007072 000206          .WORD    206          ;UNIQUE ERROR NUMBER
2652 007074 001127          .WORD    CPUERR       ;ADDRESS OF ERROR MESSAGE
2653 007076 005212          20:    INC      (R2)          ;0=0
2654 007100 001004          BNE      30          ;ERROR IF NOT 0

```



```

2655 007102 000257          CCC          ;CC=0000
2656 007104 111113          MOVB      (R1),(R3) ;405=377
2657 007106 001401          BEQ       3#        ;ERROR IF EQUAL
2658 007110 100403          BMI       4#        ;BRANCH IF GOOD
2659 007112
2660 007112 104000          3#:
2661 007114 000207          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2662 007116 001127          .WORD      207     ;UNIQUE ERROR NUMBER
2663 007120 105213          .WORD      CPUERR  ;ADDRESS OF ERROR MESSAGE
2664 007122 001373          4#:
2665          INCB      (R3) ;405=0
2666 007124 005002          BNE       3#        ;ERROR IF 405 NOT 0
2667 007126 111102          ;CHECK THAT SIGN EXTENSION OCCURS ON A MOVB TO GENERAL REGISTER.
2668 007130 100005          CLR       R2        ;INIT R2 TO ZERO.
2669 007132 102404          MOVB      (R1),R2  ;MOVE 377 TO R2
2670 007134 103403          BPL       5#        ;ERROR! BIT 15 SHOULD BE SET.
2671 007136 022702 177777          BVS       5#        ;V BIT SHOULD BE CLEARED
2672 007142 001403          BCS       5#        ;CARRY BIT SHOULD BE UNAFFECTED
2673          CMP       #177777,R2 ;TEST R2
2674          BEQ       6#        ;SIGN EXTENDED THROUGH UPPER BYTE
2675          ;ERROR! BYTE SHOULD HAVE
2676          ;SIGN EXTENDED THROUGH UPPER BYTE
2677 007144 104000          5#:
2678 007146 000210          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2679 007150 001127          .WORD      210     ;UNIQUE ERROR NUMBER
2680          .WORD      CPUERR ;ADDRESS OF ERROR MESSAGE
2681
2682 007152          6#:
2683          ;
2684          ;*****
2685          ;*TEST 70          TEST ADD MODE 1,1
2686          ;*****
2687          TST70:
2688          INC       #TESTN          ;INCREMENT TEST NUMBER
2689          MOV       #400,R4        ;R4=400
2690          MOV       #402,R1        ;R1=402
2691          MOV       #-25,(R4)     ;400=-25
2692          MOV       #24,(R1)     ;402=24
2693          ADD      (R1),(R4)     ;-25+24=-1
2694          BEQ       1#          ;ERROR IF 0
2695          BCS       1#          ;ERROR IF CARRY
2696          BPL       1#          ;ERROR IF POSITIVE RESULT
2697          INC      (R4)         ;-1+1=0
2698          BEQ       2#          ;BRANCH IF GOOD
2699          ;ERROR! CC SHOULD = 1000
2700          1#:
2701          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
2702          .WORD      211     ;UNIQUE ERROR NUMBER
2703          .WORD      CPUERR  ;ADDRESS OF ERROR MESSAGE
2704
2705          2#:
2706          ;
2707          ;*****
2708          ;*TEST 71          TEST SUB MODE 1,1
2709          ;*****
2710          TST71:

```

```

2711 007220 005267 171560      INC      #TESTN      ;INCREMENT TEST NUMBER
2712 007224 012704 000400      MOV      #400,R4      ;R4=400
2713 007230 012701 000404      MOV      #404,R1      ;R1=404
2714 007234 012714 000003      MOV      #3,(R4)      ;400-3
2715 007240 012711 000006      MOV      #6,(R1)      ;406-6
2716 007244 000277              SCC              ;CC=1111
2717 007246 161411              SUB      (R4),(R1)    ;6-3=3
2718 007250 001402              BEQ      1#           ;ERROR IF 0
2719 007252 100401              BMI      1#           ;ERROR IF MINUS
2720 007254 103003              BCC      2#           ;BRANCH IF GOOD
2721                                ;ERROR! CC SHOULD = 0000
2722 007256                                1#:
2723 007256 104000              .ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
2724 007260 000212              .WORD   212          ;UNIQUE ERROR NUMBER
2725 007262 001127              .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
2726 007264 161411              2#: SUB      (R4),(R1) ;3-3=0
2727 007266 001373              BNE      1#           ;ERROR IF NOT 0
2728
2729
2730 007270                                ;
2731                                ;MBB11:
2732                                ;*****
2733                                ;*TEST 72      TEST BIC, BIS MODE 1.1
2734                                ;*****
2735                                ;TST72:
2736 007270 005267 171510      INC      #TESTN      ;INCREMENT TEST NUMBER
2737 007274 012704 000400      MOV      #400,R4      ;R4=400
2738 007300 012701 000402      MOV      #402,R1      ;R1=402
2739 007304 012714 052525      MOV      #052525,(R4) ;400-052525
2740 007310 012711 125252      MOV      #125252,(R1) ;402-125252
2741 007314 051411              BIS      (R4),(R1)    ;R4 V R1 = -1
2742 007316 001401              BEQ      1#           ;ERROR IF 0
2743 007320 100403              BMI      2#           ;BRANCH IF GOOD
2744                                ;ERROR! CC SHOULD = 1000
2745 007322                                1#:
2746 007322 104000              .ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
2747 007324 000213              .WORD   213          ;UNIQUE ERROR NUMBER
2748 007326 001127              .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
2749 007330 005211              2#: INC      (R1)      ;402=0
2750 007332 001403              BEQ      4#           ;BRANCH IF GOOD
2751                                ;ERROR! CC SHOULD = 0100
2752 007334                                3#:
2753 007334 104000              .ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
2754 007336 000214              .WORD   214          ;UNIQUE ERROR NUMBER
2755 007340 001127              .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
2756 007342 005311              4#: DEC      (R1)      ;402=-1
2757 007344 041411              BIC      (R4),(R1)    ;R1=125252
2758 007346 001401              BEQ      5#           ;ERROR IF 0
2759 007350 100403              BMI      6#           ;BRANCH IF GOOD
2760                                ;ERROR! CC SHOULD = 1000
2761 007352                                5#:
2762 007352 104000              .ERROR   ;ALL ERRORS TO TRAP TO EMT VECTOR
2763 007354 000215              .WORD   215          ;UNIQUE ERROR NUMBER
2764 007356 001127              .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
2765 007360 005111              6#: COM      (R1)      ;402=052525
2766 007362 041114              BIC      (R1),(R4)    ;400=0
2766 007364 001403              BEQ      8#           ;BRANCH IF GOOD
    
```



```

2767
2768 007366          78:          ;ERROR! CC SHOULD = 0100
2769 007366 104000   ;ALL ERRORS TO TRAP TO EMT VECTOR
2770 007370 000216   ;UNIQUE ERROR NUMBER
2771 007372 001127   ;ADDRESS OF ERROR MESSAGE
2772 007374
2773
2774
2775 007374
2776
2777
2778
2779 007374
2780 007374 005267 171404   ;
2781 007400 012704 000400   ;*****
2782 007404 012714 052525   ;*TEST 73      TEST BIT, CMP MODE 1,1
2783 007410 012701 000402   ;*****
2784 007414 012711 125252   ;TST73:
2785 007420 000241   ;INC      $TESTN      ;INCREMENT TEST NUMBER
2786 007422 031411   ;MOV     #400,R4      ;R4=400
2787 007424 103401   ;MOV     #052525,(R4) ;400=052525
2788 007426 001403   ;MOV     #402,R1      ;R1=402
2789
2790 007430          18:          ;402=125252
2791 007430 104000   ;CLC      ;CLEAR CARRY
2792 007432 000217   ;BIT     (R4),(R1)    ;**052525+125252=0
2793 007434 001127   ;BCS     1$          ;ERROR IF CARRY
2794 007436 021411   ;BEQ     2$          ;BRANCH IF GOOD
2795 007440 001403   ;        ;ERROR! CC SHOULD = 0100
2796 007442 103002   ;
2797 007444 102001   ;
2798 007446 100403   ;
2799
2800 007450          28:          ;ALL ERRORS TO TRAP TO EMT VECTOR
2801 007450 104000   ;.WORD   217          ;UNIQUE ERROR NUMBER
2802 007452 000217   ;.WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
2803 007454 001127   ;
2804 007456 005014   ;CMP     (R4),(R1)    ;400-402=125253
2805 007460 005214   ;BEQ     3$          ;ERROR IF ZERO
2806 007462 031114   ;BCC     3$          ;ERROR IF NO CARRY
2807 007464 001403   ;BVC     3$          ;ERROR IF NO OVERFLOW
2808
2809 007466          38:          ;BRANCH IF GOOD
2810 007466 104000   ;        ;ERROR! CC SHOULD = 1000
2811 007470 000221   ;
2812 007472 001127   ;
2813 007474
2814
2815
2816 007474          48:          ;ALL ERRORS TO TRAP TO EMT VECTOR
2817
2818
2819
2820 007474          58:          ;UNIQUE ERROR NUMBER
2821 007474 005267 171304   ;ADDRESS OF ERROR MESSAGE
2822 007500 012704 000400   ;

```

2823	007504	012701	000402	MOV	#402,R1	;R1=402
2824	007510	012714	000005	MOV	#5,(R4)	;400=5
2825	007514	005021		CLR	(R1),	;402=0
2826	007516	005011		CLR	(R1)	;
2827	007520	005111		COM	(R1)	;404=-1
2828	007522	005741		TST	-(R1)	;R1=402
2829	007524	000277		SCC		;CC=1111
2830	007526	012124		MOV	(R1),,(R4),	;400=0 R4=402 R1=404
2831	007530	100403		BMI	1#	;ERROR IF MINUS
2832	007532	103002		BCC	1#	;ERROR IF NO CARRY
2833	007534	102401		BVS	1#	;ERROR IF OVERFLOW
2834	007536	001403		BEQ	2#	;BRANCH IF GOOD
2835						;ERROR! CC SHOULD= 0101
2836	007540			1#:		
2837	007540	104000		ERROR		;ALL ERRORS TO TRAP TO EMT VECTOR
2838	007542	000222		.WORD	222	;UNIQUE ERROR NUMBER
2839	007544	001127		.WORD	CPUERR	;ADDRESS OF ERROR MESSAGE
2840	007546	005244		2#:	INC	-(R4)
2841						;400=1 R4=400
2842	007550	061411		ADD	(R4),(R1)	;1# -1 =0
2843	007552	001403		BEQ	4#	;BRANCH IF GOOD
2844						;ERROR! CC SHOULD = 0100
2845	007554			3#:		
2846	007554	104000		ERROR		;ALL ERRORS TO TRAP TO EMT VECTOR
2847	007556	000223		.WORD	223	;UNIQUE ERROR NUMBER
2848	007560	001127		.WORD	CPUERR	;ADDRESS OF ERROR MESSAGE
2849	007562			4#:		
2850						
2851						
2852	007562			;		
2853				MS22:		
2854				;		
2855				*****		
2856	007562			!+TEST 75	TEST SUB MODE 2.2	
2857	007562	005267	171216	;		
2858	007566	012704	000400	TST75:		
2859	007572	012701	000402	INC	#TESTN	;INCREMENT TEST NUMBER
2860	007576	012714	177760	MOV	#400,R4	;R4=400
2861	007602	012711	177750	MOV	#402,R1	;R1=402
2862	007606	162421		MOV	#177760,(R4)	;400=177760
2863	007610	001403		MOV	#177750,(R1)	;402=177750
2864	007612	102402		SUB	(R4),,(R1),	;R1=177770
2865	007614	103001		BEQ	1#	;ERROR IF ZERO
2866	007616	100403		BVS	1#	;ERROR IF OVERFLOW
2867				BCC	1#	;ERROR IF NO CARRY
2868	007620			BMI	2#	;BRANCH IF GOOD
2869	007620	104000				;ERROR! CC SHOULD=1000
2870	007622	000224		1#:	ERROR	;ALL ERRORS TO TRAP TO EMT VECTOR
2871	007624	001127		.WORD	224	;UNIQUE ERROR NUMBER
2872	007626	005241		.WORD	CPUERR	;ADDRESS OF ERROR MESSAGE
2873	007630	162721	177771	2#:	INC	-(R1)
2874	007634	100401		SUB	#177771,(R1),	;R1=0
2875	007636	001403		BMI	3#	;ERROR IF MINUS
2876				BEQ	4#	;BRANCH IF GOOD
2877	007640					;ERROR! CCSHOULD = 0100
2878	007640	104000		3#:	ERROR	;ALL ERRORS TO TRAP TO EMT VECTOR


```

2879 007642 000225          .WORD 225          ;UNIQUE ERROR NUMBER
2880 007644 001127          .WORD CPUERR       ;ADDRESS OF ERROR MESSAGE
2881 007646
2882
2883
2884 007646
2885
2886
2887
2888 007646
2889 007646 005267 171132
2890 007652 012704 000400
2891 007656 012701 000402
2892 007662 012702 000404
2893 007666 012714 141401
2894 007672 012711 177405
2895 007676 012722 000070
2896 007702 012722 177777
2897 007706 042421
2898 007710 001401
2899 007712 100003
2900
2901 007714
2902 007714 104000
2903 007716 000226
2904 007720 001127
2905 007722 052421
2906 007724 142421
2907 007726 005301
2908 007730 152421
2909 007732 100403
2910
2911 007734
2912 007734 104000
2913 007736 000227
2914 007740 001127
2915 007742 005214
2916 007744 001403
2917
2918 007746
2919 007746 104000
2920 007750 000230
2921 007752 001127
2922 007754
2923
2924
2925 007754
2926
2927
2928
2929 007754
2930 007754 005267 171024
2931 007760 012704 000400
2932 007764 012701 000402
2933 007770 012714 125252
2934 007774 012721 100001

4$:
;
;MBC22:
;*****
; *TEST 76      TEST BIC, BICB, BIS, BISB MODE 2.2
;*****
TST76:
    INC      $TESTN          ;INCREMENT TEST NUMBER
    MOV      #400,R4         ;R4=400
    MOV      #402,R1         ;R1=402
    MOV      #404,R2         ;R2=404
    MOV      #141401,(R4)    ;400=303 001
    MOV      #177405,(R1)    ;402=377 005
    MOV      #70,(R2)+       ;404=2070
    MOV      #-1,(R2)+       ;406=-1
    BIC      (R4)+,(R1)+     ;402=074004
    BEQ      1$              ;ERROR IF ZERO
    BPL      2$              ;BRANCH IF GOOD
                          ;CC SHOULD = 1000

1$:
    ERROR
    .WORD    226              ;ALL ERRORS TO TRAP TO EMT VECTOR
                          ;UNIQUE ERROR NUMBER
    .WORD    CPUERR         ;ADDRESS OF ERROR MESSAGE
2$:
    BIS      (R4)+,(R1)+     ;404=074074
    BICB     (R4)+,(R1)+     ;406=074
    DEC      R1              ;R4=405 R1=406
    BISB     (R4)+,(R1)+     ;406=-1 R4=406 R1=407
    BMI      4$              ;BRANCH IF GOOD
                          ;406 SHOULD=-1

3$:
    ERROR
    .WORD    227              ;ALL ERRORS TO TRAP TO EMT VECTOR
                          ;UNIQUE ERROR NUMBER
    .WORD    CPUERR         ;ADDRESS OF ERROR MESSAGE
4$:
    INC      (R4)            ;406 SHOULD=0
    BEQ      6$              ;BRANCH IF GOOD
                          ;ERROR! 406 NE 0

5$:
    ERROR
    .WORD    230              ;ALL ERRORS TO TRAP TO EMT VECTOR
                          ;UNIQUE ERROR NUMBER
    .WORD    CPUERR         ;ADDRESS OF ERROR MESSAGE
6$:
;
;MBC22:
;*****
; *TEST 77      TEST BIT, CMP MODE 2.2
;*****
TST77:
    INC      $TESTN          ;INCREMENT TEST NUMBER
    MOV      #400,R4         ;R4=400
    MOV      #402,R1         ;R1=402
    MOV      #125252,(R4)    ;400=125252
    MOV      #100001,(R1)+   ;402=100001
    
```

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2935 010000 012711 100002      MOV    #100002,(R1)      ;404=100002
2936 010004 005741              TST    -(R1)            ;R1=402
2937 010006 132421              BITB   (R4)+,(R1)+     ;**ANDED RESULT= 000
2938 010010 100401              BMI    1#              ;ERROR IF MINUS
2939 010012 001403              BEQ    2#              ;BRANCH IF GOOD
2940                                ;ERROR! CC SHOULD = 0100
2941 010014              1#:
2942 010014 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
2943 010016 000231              .WORD 231                    ;UNIQUE ERROR NUMBER
2944 010020 001127              .WORD CPUERR                ;ADDRESS OF ERROR MESSAGE
2945 010022 132124              2#: BITB   (R1)+,(R4)+     ;** ANDED RESULT = 200
2946 010024 001401              BEQ    3#              ;ERROR IF EQUAL
2947 010026 100403              BMI    4#              ;BRANCH IF GOOD
2948                                ;ERROR! CC SHOULD= 1000 R4=402 R1=404
2949 010030              3#:
2950 010030 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
2951 010032 000232              .WORD 232                    ;UNIQUE ERROR NUMBER
2952 010034 001127              .WORD CPUERR                ;ADDRESS OF ERROR MESSAGE
2953 010036 022421              4#: CMP    (R4)+,(R1)+     ;RESULT =+1
2954 010040 001402              BEQ    5#              ;ERROR IF EQUAL
2955 010042 103001              BCC    5#              ;ERROR IF NO CARRY
2956 010044 100403              BMI    6#              ;BRANCH IF GOOD
2957                                ;ERROR! CC SHOULD = 0000
2958 010046              5#:
2959 010046 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
2960 010050 000233              .WORD 233                    ;UNIQUE ERROR NUMBER
2961 010052 001127              .WORD CPUERR                ;ADDRESS OF ERROR MESSAGE
2962 010054 005341              6#: DEC    -(R1)            ;404=100001
2963 010056 005741              TST    -(R1)            ;R4=404 R1=402
2964 010060 022124              CMP    (R1)+,(R4)+     ;RESULT =0
2965 010062 001403              BEQ    8#              ;BRANCH IF GOOD
2966                                ;CC SHOULD = 0100 R1=404 R4=406
2967 010064              7#:
2968 010064 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
2969 010066 000234              .WORD 234                    ;UNIQUE ERROR NUMBER
2970 010070 001127              .WORD CPUERR                ;ADDRESS OF ERROR MESSAGE
2971 010072              8#:
2972                                ;
2973                                ;MS33:
2974 010072              ;*****
2975                                ;*TEST 100      TEST SUB MODE 3,3
2976                                ;*****
2977                                ;
2978 010072              TST100:
2979 010072 005267 170706      INC    #TESTN            ;INCREMENT TEST NUMBER
2980 010076 005004              CLR    R4                ;R4=0
2981 010100 012701 000002      MOV    #2,R1             ;R1=2
2982 010104 012702 000400      MOV    #400,R2           ;R2=400
2983 010110 012714 000400      MOV    #400,(R4)         ;0=400
2984 010114 012711 000402      MOV    #402,(R1)         ;2=402
2985 010120 012722 000200      MOV    #200,(R2)+        ;400=200
2986 010124 012712 054320      MOV    #54320,(R2)       ;402=54320
2987 010130 163431              SUB    B(R4)+,B(R1)+     ;54320 - 200=54120
2988 010132 001402              BEQ    1#              ;ERROR IF ZERO
2989 010134 103401              BCS    1#              ;ERROR IF CARRY
2990 010136 100003              BPL    2#              ;BRANCH IF GOOD

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2991
2992 010140 1# : ;ERROR! CC SHOULD =0001
2993 010140 104000 ; ALL ERRORS TO TRAP TO EMT VECTOR
2994 010142 000235 ; UNIQUE ERROR NUMBER
2995 010144 001127 ; ADDRESS OF ERROR MESSAGE
2996 010146 022712 054120 2# : ; TEST R4 AUTO-INC AND RESULT
2997 010152 001403 ; BRANCH IF GOOD
2998 ; ERROR! CC SHOULD = 0100 R4=2 R1=4
2999 010154 3# : ; ALL ERRORS TO TRAP TO EMT VECTOR
3000 010154 104000 ; UNIQUE ERROR NUMBER
3001 010156 000236 ; ADDRESS OF ERROR MESSAGE
3002 010160 001127 ; RESTORE VECTORS
3003 010162 005067 167612 4# : ;
3004 010166 005067 167610 ; "
3005
3006
3007
3008 010172 ;
3009 ; MCB44:
3010 ; *****
3011 ; *TEST 101 TEST CMP, BIT MODE 4,4
3012 ; *****
3012 010172 TST101:
3013 010172 005267 170606 ; INC #TESTN ; INCREMENT TEST NUMBER
3014 010176 012704 000400 ; MOV #400,R4 ; R4=400
3015 010202 012701 000402 ; MOV #402,R1 ; R1=402
3016 010206 012721 125366 ; MOV #125366,(R1); ; 402=125366 R1=404
3017 010212 012724 173001 ; MOV #173001,(R4); ; 400=173001 R4=402
3018 010216 024441 ; CMP -(R4),-(R1) ; 173001 - 125366=045603 CC=0000
3019 010220 103401 ; BCS 1# ; ERROR IF CARRY
3020 010222 100003 ; BPL 2# ; BRANCH IF GOOD
3021 ; ; BAD COMPARE
3022 010224 1# : ; ALL ERRORS TO TRAP TO EMT VECTOR
3023 010224 104000 ; UNIQUE ERROR NUMBER
3024 010226 000237 ; ADDRESS OF ERROR MESSAGE
3025 010230 001127 ; R1=403
3026 010232 005204 2# : ; SET CARRY
3027 010234 005201 ; SEC ; 173+1=0
3028 010236 000261 ; BITB -(R1),-(R4) ; C SHOULD REMAIN SET
3029 010240 134144 ; BCC 3# ; BRANCH IF GOOD
3030 010242 103001 ; BEQ 4# ; INCORRECT COMPARE R4=400 R1=402
3031 010244 001403 ; ALL ERRORS TO TRAP TO EMT VECTOR
3032 ; UNIQUE ERROR NUMBER
3033 010246 3# : ; ADDRESS OF ERROR MESSAGE
3034 010246 104000 ; R4=402
3035 010250 000240 ; INC R1 ; R1=403
3036 010252 001127 ; INC R1 ; SET CARRY
3037 010254 005724 4# : ; BITB -(R4),-(R1) ; 173 - 173=0
3038 010256 005201 ; CMPB -(R4),-(R1) ; BRANCH IF GOOD
3039 010260 124441 ; BEQ 6# ; BAD COMPARE
3040 010262 001403 ; ALL ERRORS TO TRAP TO EMT VECTOR
3041 ; UNIQUE ERROR NUMBER
3042 010264 5# : ; ADDRESS OF ERROR MESSAGE
3043 010264 104000 ; R4=402
3044 010266 000241 ; INC R1 ; R1=403
3045 010270 001127 ; CMPB -(R4),-(R1) ; 173 - 173=0
3046 010272 6# : ; BEQ 6# ; BRANCH IF GOOD
; BAD COMPARE
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

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3103 010420          1#:
3104 010420 104000
3105 010422 000244      ERROR
3106 010424 001127      .WORD 244          ;ALL ERRORS TO TRAP TO EMT VECTOR
3107 010426 136461 000405 177772 2#: BITB 405(R4),-6(R1) ;UNIQUE ERROR NUMBER
3108 010434 001401      BEQ 3#           ;ADDRESS OF ERROR MESSAGE
3109 010436 100403      BMI 4#           ;(405)+(400)=200
3110
3111 010440          3#:
3112 010440 104000      ERROR
3113 010442 000245      .WORD 245          ;ALL ERRORS TO TRAP TO EMT VECTOR
3114 010444 001127      .WORD CPUERR      ;UNIQUE ERROR NUMBER
3115 010446          4#:
3116
3117
3118 010446          ;
3119
3120
3121
3122 010446          ;MS77:
3123 010446 005267 170332 TST104:
3124 010452 012704 000400      INC $TESTN          ;INCREMENT TEST NUMBER
3125 010456 005001      MOV #400,R4
3126 010460 012724 177776      CLR R1
3127 010464 012724 177777      MOV #-2,(R4)+      ;400=-2
3128 010470 012724 000400      MOV #-1,(R4)+      ;402=-1
3129 010474 012711 000402      MOV #400,(R4)+     ;404=400 R4=406
3130 010500 005201      MOV #402,(R1)      ;0=402
3131 010502 167471 177372 000403 INC R1              ;R1=1
3132 010510 001401      SUB #406(R4),#403(R1) ;-2 - -1 = -1
3133 010512 100403      BEQ 1#           ;ERROR IF ZERO
3134
3135 010514          1#:
3136 010514 104000      ERROR
3137 010516 000246      .WORD 246          ;ALL ERRORS TO TRAP TO EMT VECTOR
3138 010520 001127      .WORD CPUERR      ;UNIQUE ERROR NUMBER
3139 010522 167174 177777 177776 2#: SUB #1(R1),#-2(R4) ;ADDRESS OF ERROR MESSAGE
3140 010530 001403      BEQ 4#           ;-1 - -1 = 0
3141
3142 010532          3#:
3143 010532 104000      ERROR
3144 010534 000247      .WORD 247          ;ALL ERRORS TO TRAP TO EMT VECTOR
3145 010536 001127      .WORD CPUERR      ;UNIQUE ERROR NUMBER
3146 010540 005067 167234 4#: CLR 0              ;ADDRESS OF ERROR MESSAGE
3147 010544 005067 167232      CLR 2              ;RESTORE VECTORS
3148
3149
3150
3151 010550          ;
3152
3153
3154
3155 010550          ;MRLO:
3156 010550 005267 170230 TST105:
3157 010554 012704 125252      INC $TESTN          ;INCREMENT TEST NUMBER
3158 010560 000277      MOV #125252,R4     ;R4=125252
                          SCC
                          ;CC=1111

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3159 010562 006104          ROL      R4
3160 010564 102004          BVC      1#
3161 010566 103003          BCC      1#
3162 010570 022704 052525  CMP      #052525,R4
3163 010574 001403          BEQ      2#
3164
3165 010576          1#:
3166 010576 104000          ERROR
3167 010600 000250          .WORD   250
3168 010602 001127          .WORD   CPUERR
3169 010604 012704 125252 2#:  MOV      #125252,R4
3170 010610 000257          CCC
3171 010612 106104          ROLB     R4
3172 010614 103005          BCC      3#
3173 010616 102004          BVC      3#
3174 010620 100403          BMI      3#
3175 010622 022704 125124  CMP      #125124,R4
3176 010626 001403          BEQ      4#
3177
3178 010630          3#:
3179 010630 104000          ERROR
3180 010632 000251          .WORD   251
3181 010634 001127          .WORD   CPUERR
3182 010636          4#:
3183
3184
3185 010636          ;
3186          ;MRLB1:
3187          ;*****
3188          ;*TEST 106      TEST ROL, ROLB MODE 1
3189          ;*****
3190 010636 005267 170142  TST106:
3191 010642 005004          INC      #TESTN
3192 010644 012714 052525  CLR      R4
3193 010650 006114          MOV      #52525,(R4)
3194 010652 100005          ROL      (R4)
3195 010654 102004          BPL      1#
3196 010656 103403          BVC      1#
3197 010660 021427 125252  BCS      1#
3198 010664 001403          CMP      (R4),#125252
3199          BEQ      2#
3200 010666          1#:
3201 010666 104000          ERROR
3202 010670 000252          .WORD   252
3203 010672 001127          .WORD   CPUERR
3204 010674 012714 125252 2#:  MOV      #125252,(R4)
3205 010700 005204          INC      R4
3206 010702 000277          SCC
3207 010704 106114          ROLB     (R4)
3208 010706 100406          BMI      3#
3209 010710 103005          BCC      3#
3210 010712 102004          BVC      3#
3211 010714 005304          DEC      R4
3212 010716 022714 052652  CMP      #52652,(R4)
3213 010722 001403          BEQ      4#
3214
;R4=052525 WITH CARRY SET
;ERROR IF V CLEAR
;ERROR IF CARRY CLEAR
;SEE IF R0 = EXPECTED
;ERROR IF R4 NE EXPECTED
;ERROR! ROL FAILED, CC SHOULD=0011
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;R4=125252
;CC=0000
;ROTATE EVEN BYTE
;ERROR IF NO CARRY
;ERROR IF NO OVERFLOW
;ERROR IF MINUS
;SEE IF R4 = EXPECTED
;BRANCH IF GOOD
;ERROR! ROLB FAILED, CC SHOULD=1011, R4=125125
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;INCREMENT TEST NUMBER
;R4=0
;0=52525
;**TEST INSTRUCTION, 0=125252
;ERROR IF PLUS
;ERROR IF NO OVERFLOW
;ERROR IF CARRY
;SEE IF R4=EXPECTED
;BRANCH IF GOOD
;BAD ROL .CC SHOULD=1010
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;0=125252
;R4=1
;CC=1111
;**TEST INSTRUCTION
;ERROR IF RESULT IS POSITIVE
;ERROR IF NO CARRY
;ERROR IF V CLEAR
;R4=0
;ERROR IF 0 NE EXPECTED
;BRANCH IF GOOD
;ERROR! BAD ROLB ODD BYTE,CC SHOULD=1011

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3215 010724          3#:
3216 010724 104000      ERROR
3217 010726 000253      .WORD 253
3218 010730 001127      .WORD CPUERR
3219 010732          4#:
3220
3221
3222 010732          ;
3223          ;MRL2:
3224          ;*****
3225          ;*TEST 107      TEST ROL, ROLB MODE 2
3226          ;*****
3227 010732 005267 170046  TST107:
3228 010736 005004          INC      $TESTN      ;INCREMENT TEST NUMBER
3229 010740 012714 100000  CLR      R4          ;R4=0
3230 010744 000257          MOV      $100000,(R4) ;O=100000
3231 010746 006124          CCC          ;CC=0000
3232 010750 103002          ROL      (R4)+      ;*TEST INSTRUCTION
3233 010752 102001          BCC      1$         ;ERROR IF NO CARRY
3234 010754 001403          BVC      1$         ;ERROR IF NO OVERFLOW
3235          BEQ      2$         ;BRANCH IF GOOD
3236 010756          1$:
3237 010756 104000      ERROR
3238 010760 000254      .WORD 254
3239 010762 001127      .WORD CPUERR
3240 010764 005304          2$:
3241 010766 005304          DEC      R4
3242 010770 001012          DEC      R4
3243 010772 012714 004040  BNE      3$         ;ERROR IN AUTO-DEC
3244 010776 000241          MOV      $4040,(R4) ;O=4040
3245 011000 106124          CLC
3246 011002 103405          ROLB     (R4)+      ;**TEST INSTURCTION
3247 011004 102404          BCS      3$         ;ERROR IF CARRY SET
3248 011006 005304          BVS      3$         ;ERROR IF V
3249 011010 022714 004100  DEC      R4
3250 011014 001403          CMP      $04100,(R4) ;SEE IF O= EXPECTED RESULT
3251          BEQ      4$         ;BRANCH IF GOOD
3252 011016          3$:
3253 011016 104000      ERROR
3254 011020 000255      .WORD 255
3255 011022 001127      .WORD CPUERR
3256 011024          4#:
3257
3258
3259 011024          ;
3260          ;MRL3:
3261          ;*****
3262          ;*TEST 110      TEST ROL, ROLB MODE 3
3263          ;*****
3264 011024 005267 167754  TST110:
3265 011030 005004          INC      $TESTN      ;INCREMENT TEST NUMBER
3266 011032 012714 052525  CLR      R4          ;R4=0
3267 011036 000277          MOV      $052525,(R4) ;O=52525
3268 011040 006137 000000  SCC          ;CC=1111
3269 011044 100005          ROL      $00
3270 011046 102004          BPL      1$         ;**TEST INSTRUCTION MODE 3 WITH PC
          BVC      1$         ;ERROR IF PLUS
          ;ERROR IF NO OVERFLOW

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3271 011050 103403          BCS 1#          ;ERROR IF CARRY
3272 011052 022714 125253  CMP 0125253,(R4) ;COMPARE RESULT WITH EXPECTED
3273 011056 001403          BEQ 2#          ;BRANCH IF GOOD
3274                                     ;BAD ROL CC SHOULD=1010
3275 011060          1#:
3276 011060 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3277 011062 000256          .WORD 256          ;UNIQUE ERROR NUMBER
3278 011064 001127          .WORD CPUERR        ;ADDRESS OF ERROR MESSAGE
3279 011066 012714 125252  2#: MOV 0125252,(R4) ;O=125252
3280 011072 000261          SEC          ;CC=---1
3281 011074 106137 000000  ROLB 0#0        ;**TEST INSTRUCTION
3282 011100 100402          BMI 3#          ;ERROR IF MINUS
3283 011102 103001          BCC 3#          ;ERROR IF NO CARRY
3284 011104 102403          BVS 4#          ;BRANCH IF OVERFLOW
3285                                     ;ERROR! BAD ROL, CC SHOULD=1011
3286 011106          3#:
3287 011106 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3288 011110 000257          .WORD 257          ;UNIQUE ERROR NUMBER
3289 011112 001127          .WORD CPUERR        ;ADDRESS OF ERROR MESSAGE
3290 011114          4#:
3291
3292
3293 011114          ;
3294          ;MRL4:
3295          ;*****
3296          ;*TEST 111      TEST ROL MODE 4
3297          ;*****
3298          ;TST111:
3299          ;
3300          ;INC 0TESTN          ;INCREMENT TEST NUMBER
3301          ;CLR R1          ;R1=0
3302          ;MOV 02,R4          ;R4=2
3303          ;MOV 054321,(R1) ;O=54321
3304          ;SCC          ;CC=1111
3305          ;ROL -(R4)          ;**TEST INSTRUCTION
3306          ;BPL 1#          ;ERROR IF PLUS
3307          ;BVC 1#          ;ERROR IF NO OVERFLOW
3308          ;BCS 1#          ;ERROR IF CARRY
3309          ;CMP 0130643,(R1) ;SEE IF EXPECTED RESULT
3310          ;BNE 1#          ;BRANCH IF ROL FAILED
3311          ;TST R4          ;SEE IF AUTO-DEC WORKED
3312          ;BEQ 2#          ;BRANCH IF GOOD
3313          ;ERROR! BAD ROL INST
3314          ;
3315          ;
3316          ;
3317          ;
3318          ;
3319          ;
3320          ;
3321          ;
3322          ;
3323          ;
3324          ;
3325          ;
3326          ;
3327          ;
3328          ;
3329          ;
3330          ;
3331          ;
3332          ;
3333          ;
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3327 011176 012734 123456          MOV    #123456,0(R4).      ;400=123465, R4=2
3328 011202 000277                    SCC                    ;CC=1111
3329 011204 006154                    ROL    0-(R4)           ;**TEST INSTRUCTION
3330 011206 100410                    BMI    1#              ;ERROR IF RESULT IS MINUS
3331 011210 103007                    BCC    1#              ;ERROR IF NO CARRY
3332 011212 102006                    BVC    1#              ;ERROR IF NO OVERFLOW
3333 011214 005704                    TST    R4              ;SEE IF AUTO-DEC WORKED
3334 011216 001004                    BNE    1#              ;ERROR OF AUTO-DEC
3335 011220 022737 047135 000400    CMP    #47135,0#400    ;SEE IF CORRECT RESULT
3336 011226 001403                    BEQ    2#              ;BRANCH IF GOOD
3337                                     ;BAD ROL MODE 5
3338 011230                                     1#:
3339 011230 104000                    ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
3340 011232 000261                    .WORD 261                                     ;UNIQUE ERROR NUMBER
3341 011234 001127                    .WORD CPUERR                                ;ADDRESS OF ERROR MESSAGE
3342 011236                                     2#:
3343
3344
3345 011236                                     ;
3346                                     ;MRL6:
3347                                     ;*****
3348                                     ;*TEST 113      TEST ROL MODE 6
3349                                     ;*****
3350 011236 005267 167542    TST113:
3351 011242 012704 000400          INC    #TESTN          ;INCREMENT TEST NUMBER
3352 011246 005001                    MOV    #400,R4        ;R4=400
3353 011250 012711 032525          CLR    R1              ;R1=0
3354 011254 000277                    MOV    #32525,(R1)    ;0=32525
3355 011256 006164 177400          SCC                    ;
3356 011262 100405                    ROL    -400(R4)       ;**TEST INSTRUCTION
3357 011264 103404                    BMI    1#              ;ERROR IF MINUS
3358 011266 102403                    BCS    1#              ;ERROR IF CARRY
3359 011270 022711 065253          BVS    1#              ;ERROR IF OVERFLOW
3360 011274 001403                    CMP    #65253,(R1)    ;SEE IF CORRECT RESULT
3361                                     BEQ    2#              ;BRANCH IF GOOD
3362 011276                                     ;BAD ROL MODE 6
3363 011276 104000                    1#:
3364 011300 000262                    ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
3365 011302 001127                    .WORD 262                                     ;UNIQUE ERROR NUMBER
3366 011304                    .WORD CPUERR                                ;ADDRESS OF ERROR MESSAGE
3367                                     2#:
3368
3369 011304                                     ;
3370                                     ;MRL7:
3371                                     ;*****
3372                                     ;*TEST 114      TEST ROL MODE 7
3373                                     ;*****
3374 011304 005267 167474    TST114:
3375 011310 012704 000400          INC    #TESTN          ;INCREMENT TEST NUMBER
3376 011314 005037 000402          MOV    #402,R4        ;R4=400
3377 011320 012737 100000 000000    CLR    #402           ;402=0
3378 011326 006174 000002          MOV    #100000,0#0    ;0=100000
3379 011332 100406                    ROL    02(R4)         ;**TEST INSTRUCTION
3380 011334 001005                    BMI    1#              ;ERROR IF MINUS
3381 011336 103004                    BNE    1#              ;ERROR IF NOT ZERO
3382 011340 102003                    BCC    1#              ;ERROR IF NO CARRY
                                     BVC    1#              ;ERROR IF NO OVERFLOW

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3383 011342 005737 000000          TST      000
3384 011346 001403                BEQ      20          ;CHECK RESULT
3385                                     ;BRANCH IF GOOD
3386                                     ;BAD ROL MODE 7
3387 011350          10:          ERROR
3388 011352 104000          .WORD
3389 011354 000263          .WORD      263
3390 011356          20:          CPUERR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3391                                     ;UNIQUE ERROR NUMBER
3392                                     ;ADDRESS OF ERROR MESSAGE
3393 011356          ;
3394          ;MSW37:
3395          ;*****
3396          ;*TEST 115      TEST SWAB MODE 37
3397          ;*****
3398 011356 005267 167422          TST115:
3399 011362 012704 000400          INC      0TESTN          ;INCREMENT TEST NUMBER
3400 011366 012714 040700          MOV      0400,R4          ;R4=400
3401 011372 000337 000400          MOV      040700,(R4)     ;400= 101 300
3402 011376 100406          SWAB     00400           ;400 SHOULD = 300 101
3403 011400 022714 140101          BMI     10              ;ERROR IF MINUS
3404 011404 001003          CMP      0140101,(R4)    ;SEE IF EXPECTED RESULT
3405 011406 000337 000400          BNE     10              ;BRANCH IF BAD
3406 011412 100403          SWAB     00400           ;400=101 300
3407          BMI     20              ;BRANCH IF GOOD
3408          ;ERROR! BAD SWAB MODE 37
3409 011414          10:          ERROR
3410 011416 104000          .WORD
3411 011420 000264          .WORD      264
3412 011422          20:          CPUERR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3413                                     ;UNIQUE ERROR NUMBER
3414                                     ;ADDRESS OF ERROR MESSAGE
3415 011422          ;
3416          ;MRR0:
3417          ;*****
3418          ;*TEST 116      TEST ROR MODE 0
3419          ;*****
3420 011422 005267 167356          TST116:
3421 011426 012704 052525          INC      0TESTN          ;INCREMENT TEST NUMBER
3422 011432 000257          MOV      052525,R4       ;R4=52525
3423 011434 006004          CCC
3424 011436 103003          ROR      R4              ;CC=0000
3425 011440 022704 025252          BCC     10              ;R4 SHOULD = 25252 WITH CARRY
3426 011444 001403          CMP      025252,R4       ;ERROR IF NO CARRY
3427          BEQ      20              ;SEE IF R4= EXPECTED
3428          ;BRANCH IF GOOD
3429          ;ROR MODE 0 FAILED
3430 011450          10:          ERROR
3431 011452 104000          .WORD
3432 011454 000265          .WORD      265
3433          CPUERR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3434                                     ;UNIQUE ERROR NUMBER
3435          ;ADDRESS OF ERROR MESSAGE
3436          ;
3437          ;MRRB1:
3438          ;*****
3439          ;*TEST 117      TEST RORB MODE 1
3440          ;*****

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3439 011454          TST117:
3440 011454 005267 167324      INC      #TESTN      ;INCREMENT TEST NUMBER
3441 011460 005004          CLR      R4          ;R4=0
3442 011462 012714 000001      MOV      #1,(R4)    ;O=1
3443 011466 000277          SCC          ;CC=1111
3444 011470 106014          RORB     (R4)        ;O=000200, NO C
3445 011472 103004          BCC     1#          ;ERROR IF NO CARRY
3446 011474 100003          BPL     1#          ;ERROR IF PLUS
3447 011476 022714 000200      CMP      #200,(R4)  ;CHECK RESULT
3448 011502 001403          BEQ     2#          ;BRANCH IF GOOD
3449
3450 011504          1#:
3451 011504 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3452 011506 000266          .WORD 266      ;UNIQUE ERROR NUMBER
3453 011510 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
3454 011512          2#:
3455
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3458 011512          MJ:
3459
3460          ;*****
3461          ;*TEST 120      TEST JMP - ALL MODES
3462          ;*****
3463 011512 005267 167266          TST120:      INC      #TESTN      ;INCREMENT TEST NUMBER
3464 011516 012737 000001 001066      MOV      #1,#SEQ    ;SETUP TEST SEQUENCER
3465 011524 012701 011600          MOV      #MJU1,R1   ;SET MODE 1 JUMP ADDRESS
3466 011530 000111          JMP      (R1)        ;*JMP MODE 1
3467 011532 023727 001066 000002      MJU2:      CMP      #SEQ,#2    ;CHECK FOR CORRECT SEQUENCE
3468 011540 001403          BEQ     MJU2A        ;BRANCH IF GOOD
3469
3470 011542          1#:
3471 011542 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3472 011544 000267          .WORD 267      ;UNIQUE ERROR NUMBER
3473 011546 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
3474
3475 011550 020127 011534          MJU2A:     CMP      R1,#MJU2+2 ;CHECK FOR AUTO-INCREMENT
3476 011554 001403          BEQ     MJU2B        ;BRANCH IF GOOD
3477
3478 011556          2#:
3479 011556 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3480 011560 000270          .WORD 270      ;UNIQUE ERROR NUMBER
3481 011562 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
3482
3483 011564 005237 001066          MJU2B:     INC      #SEQ      ;UPDATE TEST SEQUENCER
3484 011570 012701 011576          MOV      #MJ2,R1    ;SETUP MODE 3 JUMP
3485 011574 000131          JMP      @R1        ;JMP MODE 3
3486 011576 011630          MJ2:      .WORD MJU3        ;MODE 3 DESTINATION
3487 011600 023727 001066 000001      MJU1:      CMP      #SEQ,#1    ;TEST FOR CORRECT SEQUENCE
3488 011606 001403          BEQ     MJU1A        ;BRANCH IF GOOD
3489
3490 011610          3#:
3491 011610 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
3492 011612 000271          .WORD 271      ;UNIQUE ERROR NUMBER
3493 011614 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
3494

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3495	011616	005237	001066		MJU1A:	INC	0#SEQ		;UPDATE SEQUENCE
3496	011622	012701	011532			MOV	0MJU2,R1		;SETUP MODE 2 DESTINATION
3497	011626	000121				JMP	(R1)+		;JUMP MODE 2
3498	011630	023727	001066	000003	MJU3:	CMP	0#SEQ,#3		;TEST FOR CORRECT SEQUENCE
3499	011636	001403				BEQ	MJU3A		;BRANCH IF GOOD
3500									;ERROR! JMP OUT OF SEQUENCE
3501	011640				4:				
3502	011640	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
3503	011642	000272				.WORD	272		;UNIQUE ERROR NUMBER
3504	011644	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
3505									
3506	011646	022701	011600		MJU3A:	CMP	0MJ2+2,R1		;TEST AUTO-INCREMENT
3507	011652	001403				BEQ	MJU3B		;BRANCH IF GOOD
3508									;ERROR! AUTO-INCREMENT FAILED MODE 3
3509	011654				5:				
3510	011654	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
3511	011656	000273				.WORD	273		;UNIQUE ERROR NUMBER
3512	011660	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
3513									
3514	011662	005237	001066		MJU3B:	INC	0#SEQ		;UPDATE SEQUENCER
3515	011666	012701	011746			MOV	0MJU4+2,R1		;SETUP DESTINATION MODE 4
3516	011672	000141				JMP	-(R1)		;EXECUTE JUMP MODE 4
3517	011674	000000			MJU5:	HALT			
3518	011676	022701	012012			CMP	0MJ5,R1		;CHECK AUTO-DECREMENT
3519	011702	001403				BEQ	MJU5A		;BRANCH IF GOOD AUTO-DEC
3520									;ERROR! AUTO-DEC FAILED MODE 5
3521	011704				6:				
3522	011704	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
3523	011706	000274				.WORD	274		;UNIQUE ERROR NUMBER
3524	011710	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
3525									
3526	011712	023727	001066	000005	MJU5A:	CMP	0#SEQ,#5		;TEST CORRECT SEQUENCE
3527	011720	001403				BEQ	MJU5B		;BRANCH IF GOOD SEQUENCE
3528									;ERROR! JMP OUT OF SEQUENCE
3529	011722				7:				
3530	011722	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
3531	011724	000275				.WORD	275		;UNIQUE ERROR NUMBER
3532	011726	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
3533									
3534	011730	005237	001066		MJU5B:	INC	0#SEQ		;UPDATE SEQUENCE COUNT
3535	011734	012701	012007			MOV	0MJU6-5,R1		;SETUP DESTINATION MODE6
3536	011740	000161	000005			JMP	+5(R1)		;JUMP MODE 6
3537									
3538	011744	000240			8:				
3539	011746	022701	011744		MJU4:	NOP			;TEST AUTO-DECR
3540	011752	001403				CMP	0MJU4,R1		;BRANCH IF GOOD
3541						BEQ	MJU4A		;ERROR! MODE 4 AUTO-DEC FAILED
3542	011754				8:				
3543	011754	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
3544	011756	000276				.WORD	276		;UNIQUE ERROR NUMBER
3545	011760	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
3546									
3547	011762	023727	001066	000004	MJU4A:	CMP	0#SEQ,#4		;TEST FOR CORRECT SEQUENCE
3548	011770	001403				BEQ	MJU4B		;BRANCH IF CORRECT SEQUENCE
3549									;ERROR! INCORRECT JMP SEQUENCE
3550	011772				9:				


```

3551 011772 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
3552 011774 000277          .WORD        277          ; UNIQUE ERROR NUMBER
3553 011776 001127          .WORD        CPUERR       ; ADDRESS OF ERROR MESSAGE
3554
3555 012000 005237 001066    MJU4B: INC      @#SEQ       ; UPDATE SEQUENCE
3556 012004 012701 012014    MOV      @MJ5+2,R1       ; SETUP MODE 5 POINTER
3557 012010 000151          JMP      @-(R1)         ; EXECUTE MODE 5 JMP
3558
3559 012012 011676          ; MJ5:  .WORD        MJU5+2 ; POINTER MODE 5
3560
3561 012014 022737 000006 001066    MJU6: CMP      @6,@#SEQ   ; CHECK FOR CORRECT SEQUENCE
3562 012022 001403          BEQ      MJU6A          ; BRANCH IF GOOD
3563
3564 012024          10#:
3565 012024 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
3566 012026 000300          .WORD        300          ; UNIQUE ERROR NUMBER
3567 012030 001127          .WORD        CPUERR       ; ADDRESS OF ERROR MESSAGE
3568
3569 012032 005237 001066    MJU6A: INC      @#SEQ       ; UPDATE SEQUENCER
3570 012036 012701 012056    MOV      @MJ7+10,R1     ; SETUP INDEX
3571 012042 000171 177770    JMP      @-10(R1)      ; EXECUTE MODE 7 JUMP
3572 012046 012052          MJ7:  .WORD        MJU7    ; POINTER FOR MODE 7
3573 012050 000000          HALT
3574 012052 022737 000007 001066    MJU7: CMP      @7,@#SEQ   ; TEST FOR CORRECT SEQUENCE
3575 012060 001403          BEQ      MJU7E          ; BRANCH IF GOOD SEQUENCE
3576
3577 012062          11#:
3578 012062 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
3579 012064 000301          .WORD        301          ; UNIQUE ERROR NUMBER
3580 012066 001127          .WORD        CPUERR       ; ADDRESS OF ERROR MESSAGE
3581
3582 012070          MJU7E:
3583
3584
3585
3586
3587
3588 012070          ; *****
3589 012070 005267 166710    TST121: INC      @TESTN        ; INCREMENT TEST NUMBER
3590 012074 012701 012404    MOV      @128,R1       ; SET UP R1 WITH ADDRESS OF ERROR
3591
3592 012100 012717          MOV      (PC)+,(PC)    ; ROUTINE
3593 012102 000240          .WORD        NOP        ; WRITE THE NOP OVER THE JMP INSTRUCTION
3594 012104 000111          64#: .WORD        111    ; NOP INSTRUCTION
3595 012106 012717          MOV      (PC)+,(PC)    ; WRITE THE NOP OVER THE JMP INSTRUCTION
3596 012110 000240          .WORD        NOP        ; NOP INSTRUCTION
3597 012112 000111          65#: .WORD        111    ; JMP (R1)
3598 012114 012717          MOV      (PC)+,(PC)    ; WRITE THE NOP OVER THE JMP INSTRUCTION
3599 012116 000240          .WORD        NOP        ; NOP INSTRUCTION
3600 012120 000111          66#: .WORD        111    ; JMP (R1)
3601 012122 012717          MOV      (PC)+,(PC)    ; WRITE THE NOP OVER THE JMP INSTRUCTION
3602 012124 000240          .WORD        NOP        ; NOP INSTRUCTION
3603 012126 000111          67#: .WORD        111    ; JMP (R1)
3604 012130 012717          MOV      (PC)+,(PC)    ; WRITE THE NOP OVER THE JMP INSTRUCTION
3605 012132 000240          .WORD        NOP        ; NOP INSTRUCTION
3606 012134 000111          68#: .WORD        111    ; JMP (R1)

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3607	012136	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3608	012140	000240		.WORD	NOP		;NOP INSTRUCTION
3609	012142	000111	69:	.WORD	111		;JMP (R1)
3610	012144	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3611	012146	000240		.WORD	NOP		;NOP INSTRUCTION
3612	012150	000111	70:	.WORD	111		;JMP (R1)
3613	012152	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3614	012154	000240		.WORD	NOP		;NOP INSTRUCTION
3615	012156	000111	71:	.WORD	111		;JMP (R1)
3616	012160	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3617	012162	000240		.WORD	NOP		;NOP INSTRUCTION
3618	012164	000111	72:	.WORD	111		;JMP (R1)
3619	012166	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3620	012170	000240		.WORD	NOP		;NOP INSTRUCTION
3621	012172	000111	73:	.WORD	111		;JMP (R1)
3622	012174	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3623	012176	000240		.WORD	NOP		;NOP INSTRUCTION
3624	012200	000111	74:	.WORD	111		;JMP (R1)
3625	012202	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3626	012204	000240		.WORD	NOP		;NOP INSTRUCTION
3627	012206	000111	75:	.WORD	111		;JMP (R1)
3628	012210	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3629	012212	000240		.WORD	NOP		;NOP INSTRUCTION
3630	012214	000111	76:	.WORD	111		;JMP (R1)
3631	012216	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3632	012220	000240		.WORD	NOP		;NOP INSTRUCTION
3633	012222	000111	77:	.WORD	111		;JMP (R1)
3634	012224	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3635	012226	000240		.WORD	NOP		;NOP INSTRUCTION
3636	012230	000111	78:	.WORD	111		;JMP (R1)
3637	012232	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3638	012234	000240		.WORD	NOP		;NOP INSTRUCTION
3639	012236	000111	79:	.WORD	111		;JMP (R1)
3640	012240	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3641	012242	000240		.WORD	NOP		;NOP INSTRUCTION
3642	012244	000111	80:	.WORD	111		;JMP (R1)
3643	012246	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3644	012250	000240		.WORD	NOP		;NOP INSTRUCTION
3645	012252	000111	81:	.WORD	111		;JMP (R1)
3646	012254	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3647	012256	000240		.WORD	NOP		;NOP INSTRUCTION
3648	012260	000111	82:	.WORD	111		;JMP (R1)
3649	012262	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3650	012264	000240		.WORD	NOP		;NOP INSTRUCTION
3651	012266	000111	83:	.WORD	111		;JMP (R1)
3652	012270	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3653	012272	000240		.WORD	NOP		;NOP INSTRUCTION
3654	012274	000111	84:	.WORD	111		;JMP (R1)
3655	012276	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3656	012300	000240		.WORD	NOP		;NOP INSTRUCTION
3657	012302	000111	85:	.WORD	111		;JMP (R1)
3658	012304	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3659	012306	000240		.WORD	NOP		;NOP INSTRUCTION
3660	012310	000111	86:	.WORD	111		;JMP (R1)
3661	012312	012717		MOV	(PC)+,(PC)		;WRITE THE NOP OVER THE JMP INSTRUCTION
3662	012314	000240		.WORD	NOP		;NOP INSTRUCTION


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3663 012316 000111      874:  .WORD 111          ;JMP (R1)
3664 012320 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3665 012322 000240      .WORD NOP          ;NOP INSTRUCTION
3666 012324 000111      884:  .WORD 111          ;JMP (R1)
3667 012326 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3668 012330 000240      .WORD NOP          ;NOP INSTRUCTION
3669 012332 000111      894:  .WORD 111          ;JMP (R1)
3670 012334 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3671 012336 000240      .WORD NOP          ;NOP INSTRUCTION
3672 012340 000111      904:  .WORD 111          ;JMP (R1)
3673 012342 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3674 012344 000240      .WORD NOP          ;NOP INSTRUCTION
3675 012346 000111      914:  .WORD 111          ;JMP (R1)
3676 012350 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3677 012352 000240      .WORD NOP          ;NOP INSTRUCTION
3678 012354 000111      924:  .WORD 111          ;JMP (R1)
3679 012356 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3680 012360 000240      .WORD NOP          ;NOP INSTRUCTION
3681 012362 000111      934:  .WORD 111          ;JMP (R1)
3682 012364 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3683 012366 000240      .WORD NOP          ;NOP INSTRUCTION
3684 012370 000111      944:  .WORD 111          ;JMP (R1)
3685 012372 012717      MOV (PC)+,(PC)      ;WRITE THE NOP OVER THE JMP INSTRUCTION
3686 012374 000240      .WORD NOP          ;NOP INSTRUCTION
3687 012376 000111      954:  .WORD 111          ;JMP (R1)
3688 012400 000137      JMP 001290          ;JUMP OVER ERROR CALL
3689 012404                1284:                ;ERROR! PRE-FETCH BUFFER WAS NOT
3690                                ;OVER WRITTEN
3691 012404 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
3692 012406 000302                .WORD 302            ;UNIQUE ERROR NUMBER
3693 012410 001127                .WORD CPUERR        ;ADDRESS OF ERROR MESSAGE
3694                                ;
3695                                ;
3696                                ; NOW RESTORE THE OVER WRITTEN JMP INSTRUCTIONS FOR THE NEXT PASS.
3697 012412 012702 000040      1294:  MOV 032,R2          ;SET UP R2 AS COUNTER
3698 012416 012703 012104      MOV 064,R3          ;SET UP R3 AS POINTER
3699 012422 012713 000111      1304:  MOV 0111,(R3)       ;RESTORE OVER WRITTEN JUMPS
3700 012426 062703 000006      ADD 06,R3           ;POINT TO NEXT OVER WRITTEN ADDR.
3701 012432 077205                SOB R2,1304         ;DO UNTIL R2=0
3702
3703
3704 012434                ;
3705                ; MJP:
3706                ;*****
3707                ;*TEST 122 TEST JMP MODES 17,27,37,67,77*
3708                ;*****
3709 012434 005267 166344      TST122:            INC 0TESTN          ;INCREMENT TEST NUMBER
3710 012440 012737 000000      MOV 00,00SEQ        ;SETUP TEST SEQUENCER
3711 012446 000117                JMP (R7)            ;JUMP MODE 17(SHOULD BE IN-LINE)
3712
3713 012450 005737 001066      ; MJP17:           TST 00SEQ           ;CHECK SEQUENCE
3714 012454 001403                BEQ 20              ;BRANCH IF GOOD
3715                                ;ERROR! BAD JUMP
3716 012456                14:                ;
3717 012456 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
3718 012460 000303                .WORD 303            ;UNIQUE ERROR NUMBER

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3775
3776
3777 012624
3778
3779
3780
3781 012624
3782 012624 005267 166154
3783 012630 010637 001070
3784 012634 010637 001072
3785 012640 162737 000002 001072
3786 012646 012737 000001 001066
3787 012654 012701 012760
3788 012660 005004
3789 012662 005104
3790 012664 004411
3791
3792 012666 022737 000002 001066
3793 012674 001403
3794
3795 012676
3796 012676 104000
3797 012700 000310
3798 012702 001127
3799
3800 012704 023706 001072
3801 012710 001006
3802 012712 021627 125252
3803 012716 001003
3804 012720 022704 013050
3805 012724 001403
3806
3807 012726
3808 012726 104000
3809 012730 000311
3810 012732 001127
3811
3812 012734 005237 001066
3813 012740 013706 001070
3814 012744 012701 012756
3815 012750 005004
3816 012752 004431
3817 012754 000000
3818 012756 013144
3819
3820 012760 022737 000001 001066
3821 012766 001403
3822
3823 012770
3824 012770 104000
3825 012772 000312
3826 012774 001127
3827
3828 012776 023706 001072
3829 013002 001006
3830 013004 021627 177777

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;
;
; MJSR:
;*****
; *TEST 123 TEST JSR ALL MODES
;*****
TST123:
      INC      #TESTN           ; INCREMENT TEST NUMBER
      MOV      R6,#SPSJ        ; SAVE STACK POINTER LOCATION
      MOV      R6,#SPSJ
      SUB      #2,#SPSJ        ; SPSJ = R6 AFTER DECREMENT
      MOV      #1,#SEQ         ; SETUP SEQUENCE COUNTER
      MOV      #MJSR1,R1       ; SETUP INITIAL JUMP IN MODE 1
      CLR      R4
      COM      R4
      JSR      R4,(R1)         ; R4=-1 TO BE SAVED ON STACK
                                  ; JSR MODE 1
;
; MJSR2:
      CMP      #2,#SEQ         ; TEST FOR CORRECT SEQUENCE
      BEQ      MJSR2A          ; BRANCH IF GOOD
                                  ; ERROR! MODE 2 JUMPED TO OUT OF SEQUENCE
5$:
      ERROR   .WORD 310        ; ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   CPUERR          ; UNIQUE ERROR NUMBER
                                  ; ADDRESS OF ERROR MESSAGE
;
; MJSR2A:
      CMP      #SPSJ,R6        ; VERIFY STACK DECREMENT
      BNE      6$              ; BRANCH IF STACK INCORRECT
      CMP      (R6),#125252    ; VERIFY CONTENTS OF STACK
      BNE      6$              ; BRANCH IF DATA ON STACK INCORRECT
      CMP      #MJSR4,R4      ; SEE IF CORRECT RETURN ADDRESS
      BEQ      MJSR2B          ; BRANCH IF GOOD
                                  ; ERROR! JSR MODE 2 FAILED
6$:
      ERROR   .WORD 311        ; ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   CPUERR          ; UNIQUE ERROR NUMBER
                                  ; ADDRESS OF ERROR MESSAGE
;
; MJSR2B:
      INC      #SEQ            ; UPDATE SEQUENCE COUNTER
      MOV      #SPS,R6        ; RELOAD STACK POINTER
      MOV      #MJSRA,R1      ; SETUP JSR MODE 3
      CLR      R4
      JSR      R4,#(R1)       ; DIFFERENT DATA TO R4
                                  ; JSR MODE 3
;
; MJSRA:
      .WORD   MJSR3           ; LITERAL FOR JUMP MODE 3
;
; MJSR1:
      CMP      #1,#SEQ         ; TEST FOR CORRECT SEQUENCE
      BEQ      MJSR1A          ; BRANCH IF GOOD
                                  ; ERROR! MODE 1 JUMPED TO OUT OF SEQUENCE
7$:
      ERROR   .WORD 312        ; ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   CPUERR          ; UNIQUE ERROR NUMBER
                                  ; ADDRESS OF ERROR MESSAGE
;
; MJSR1A:
      CMP      #SPSJ,R6        ; VERIFY STACK DECREMENT
      BNE      8$              ; BRANCH IF STACK INCORRECT
      CMP      (R6),#-1       ; VERIFY CONTENT OF STACK

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3831	013010	001003				BNE	8:		; BRANCH IF DATA ON STACK INCORRECT
3832	013012	022704	012666			CMP		#MJSR2,R4	; SEE IF CORRECT RETURN ADDRESS
3833	013016	001403				BEQ		MJSR1B	; BRANCH IF GOOD
3834									; ERROR! JSR MODE 2 FAILED
3835	013020				8:				
3836	013020	104000				ERROR			; ALL ERRORS TO TRAP TO EMT VECTOR
3837	013022	000313				.WORD		313	; UNIQUE ERROR NUMBER
3838	013024	001127				.WORD		CPUERR	; ADDRESS OF ERROR MESSAGE
3839									
3840	013026	005237	001066		MJSR1B:	INC		#0SEQ	; UPDATE SEQUENCE COUNTER
3841	013032	013706	001070			MOV		#0SPS,R6	; RELOAD STACK POINTER
3842	013036	012704	125252			MOV		#125252,R4	; SETUP R4 DATA
3843	013042	012701	012666			MOV		#MJSR2,R1	; SETUP MODE 2 JUMP ADDRESS
3844	013046	004421				JSR		R4,(R1)	; *JUMP MODE 2
3845									
3846									
3847	013050	022737	000004	001066	MJSR4:	CMP		#4,#0SEQ	; TEST FOR CORRECT SEQUENCE
3848	013056	001403				BEQ		MJSR4A	; BRANCH IF GOOD
3849									; ERROR! MODE 4 JUMPED TO OUT OF SEQUENCE
3850	013060				9:				
3851	013060	104000				ERROR			; ALL ERRORS TO TRAP TO EMT VECTOR
3852	013062	000314				.WORD		314	; UNIQUE ERROR NUMBER
3853	013064	001127				.WORD		CPUERR	; ADDRESS OF ERROR MESSAGE
3854									
3855	013066	023706	001072		MJSR4A:	CMP		#0SPSJ,R6	; VERIFY STACK DECREMENT
3856	013072	001006				BNE		10:	; BRANCH IF STACK INCORRECT
3857	013074	021627	052525			CMP		(R6),#052525	; VERIFY CONTENTS OF STACK
3858	013100	001003				BNE		10:	; BRANCH IF DATA ON STACK INCORRECT
3859	013102	022704	013236			CMP		#MJSR6,R4	; SEE IF CORRECT RETURN ADDRESS
3860	013106	001403				BEQ		MJSR4B	; BRANCH IF GOOD
3861									; ERROR! JSR MODE 4 FAILED
3862	013110				10:				
3863	013110	104000				ERROR			; ALL ERRORS TO TRAP TO EMT VECTOR
3864	013112	000315				.WORD		315	; UNIQUE ERROR NUMBER
3865	013114	001127				.WORD		CPUERR	; ADDRESS OF ERROR MESSAGE
3866									
3867	013116	005237	001066		MJSR4B:	INC		#0SEQ	; UPDATE SEQUENCE COUNTER
3868	013122	013706	001070			MOV		#0SPS,R6	; RELOAD STACK POINTER
3869	013126	012704	000377			MOV		#377,R4	; SETUP R4 DATA
3870	013132	012701	013144			MOV		#MJSRB+2,R1	; SETUP JSR VECTOR
3871	013136	004451				JSR		R4,#-(R1)	; JSR MODE 5
3872	013140	000000				HALT			
3873	013142	013332			MJSRB:	.WORD		MJSR5	; MODE 5 VECTOR
3874									
3875									
3876	013144	022737	000003	001066	MJSR3:	CMP		#3,#0SEQ	; TEST FOR CORRECT SEQUENCE
3877	013152	001403				BEQ		MJSR3A	; BRANCH IF GOOD
3878									; ERROR! MODE 3 JUMPED TO OUT OF SEQUENCE
3879	013154				11:				
3880	013154	104000				ERROR			; ALL ERRORS TO TRAP TO EMT VECTOR
3881	013156	000316				.WORD		316	; UNIQUE ERROR NUMBER
3882	013160	001127				.WORD		CPUERR	; ADDRESS OF ERROR MESSAGE
3883									
3884	013162	023706	001072		MJSR3A:	CMP		#0SPSJ,R6	; VERIFY STACK DECREMENT
3885	013166	001006				BNE		12:	; BRANCH IF STACK INCORRECT
3886	013170	021627	000000			CMP		(R6),#0	; VERIFY CONTENTS OF STACK


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3943 013362 001003          BNE      16#
3944 013364 022704 013140  CMP      @MJSRB-2,R4
3945 013370 001403          BEQ      MJSR5B
3946
3947 013372          16#:
3948 013372 104000          ERROR
3949 013374 000323          .WORD   323
3950 013376 001127          .WORD   CPUERR
3951
3952 013400 005237 001066  MJSR5B: INC      @#SEQ
3953 013404 013706 001070  MOV      @#SPS,R6
3954 013410 012704 123456  MOV      @123456,R4
3955 013414 012701 013246  MOV      @MJSR6+10,R1
3956 013420 004461 177770  JSR      R4,-10(R1)
3957
3958
3959 013424 022737 000007 001066  MJSR7:  CMP      @7,@#SEQ
3960 013432 001403          BEQ      MJSR7A
3961
3962 013434          17#:
3963 013434 104000          ERROR
3964 013436 000324          .WORD   324
3965 013440 001127          .WORD   CPUERR
3966
3967 013442 023706 001072  MJSR7A: CMP      @#SPSJ,R6
3968 013446 001006          BNE      18#
3969 013450 021627 177773  CMP      (R6),@-5
3970 013454 001003          BNE      18#
3971 013456 022704 013330  CMP      @MJSR5-2,R4
3972 013462 001403          BEQ      MJSR7E
3973
3974 013464          18#:
3975 013464 104000          ERROR
3976 013466 000325          .WORD   325
3977 013470 001127          .WORD   CPUERR
3978
3979 013472          MJSR7E:
3980 013472 013706 001070  MOV      @#SPS,R6
3981
3982
3983 013476          MIRA:
3984
3985          ;*****
3986          ;*TEST 124      TEST JSR MODES 27, 37, 67, 77
3987          ;*****
3988          TST124:
3989 013476 005267 165302          INC      @TESTN
3990 013502 012737 000001 001066  MOV      @1,@#SEQ
3991 013510 010637 001070  MOV      R6,@#SPS
3992 013514 010637 001072  MOV      R6,@#SPSJ
3993 013520 162737 000002 001072  SUB      @2,@#SPSJ
3994 013526 012704 177777  MOV      @-1,R4
3995 013532 004427 000240  JSR      R4,@240
3996
3996 013536 022737 000001 001066  MJR27:  CMP      @1,@#SEQ
3997 013544 001011          BNE      1#
3998 013546 023706 001072  CMP      @#SPSJ,R6

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;BRANCH IF DATA ON STACK INCORRECT
;SEE IF CORRECT RETURN ADDRESS
;BRANCH IF GOOD
;ERROR! JSR MODE 5 FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;UPDATE SEQUENCE COUNTER
;RELOAD STACK POINTER
;SETUP DATA IN R4
;SETUP JSR VECTOR
;JUMP MODE 6

; TEST FOR CORRECT SEQUENCE
;BRANCH IF GOOD
;ERROR! MODE 7 JUMPED TO OUT OF SEQUENCE

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;VERIFY STACK DECIMENT
;BRANCH IF STACK INCORRECT
;VERIFY CONTENTS OF STAACK
;BRANCH IF DATA ON STACK INCORRECT
;SEE IF CORRECT RETURN ADDRESS
;BRANCH IF GOOD
;ERROR! JSR MODE 7 FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;REPLACE STACK

;INCREMENT TEST NUMBER
;SETUP SEQUENCER
;SAVE STACK ADDRESS
;SAVE STACK DECIMENT ADDRESS
;
;SETUP R4 DATA
;EXECUTE A JSR MODE 27

;VERIFY COERRECT TEST SEQUENCE
;INCORRECT TEST SEQUENCE
;VERIFY STACK POINTER

3999	013552	001006			BNE	1#		
4000	013554	021627	177777		CMP	(R6),#-1		
4001	013560	001003			BNE	1#		
4002	013562	020427	013536		CMP	R4,#MJR27		
4003	013566	001403			BEQ	MJR27A		
4004								
4005	013570							
4006	013570	104000			1#:			
4007	013572	000326			ERROR			
4008	013574	001127			.WORD	326		
4009					.WORD	CPUERR		
4010	013576	005237	001066		MJR27A:	INC	0#SEQ	
4011	013602	012704	152525		MOV	0152525,R4		
4012	013606	013706	001070		MOV	0#SPS,R6		
4013	013612	004437	013704		JSR	R4,0#MJR37		
4014	013616	000000			MJR27B:	HALT		
4015								
4016	013620	023727	001066	000003	MJR67:	CMP	0#SEQ,#3	
4017	013626	001011			BNE	2#		
4018	013630	023706	001072		CMP	0#SPSJ,R6		
4019	013634	001006			BNE	2#		
4020	013636	021627	000125		CMP	(R6),#125		
4021	013642	001003			BNE	2#		
4022	013644	020427	013764		CMP	R4,#MJR77		
4023	013650	001403			BEQ	MJR67A		
4024								
4025	013652				2#:			
4026	013652	104000			ERROR			
4027	013654	000327			.WORD	327		
4028	013656	001127			.WORD	CPUERR		
4029								
4030	013660	005237	001066		MJR67A:	INC	0#SEQ	
4031	013664	013706	001070		MOV	0#SPS,R6		
4032	013670	012704	000001		MOV	#1,R4		
4033	013674	004477	000002		JSR	R4,0#MJR68		
4034	013700	000000			MJR6A:	HALT		
4035	013702	013764			MJR6B:	.WORD	MJR77	
4036								
4037	013704	023727	001066	000002	MJR37:	CMP	0#SEQ,#2	
4038	013712	001011			BNE	2#		
4039	013714	023706	001072		CMP	0#SPSJ,R6		
4040	013720	001006			BNE	2#		
4041	013722	021627	152525		CMP	(R6),#152525		
4042	013726	001003			BNE	2#		
4043	013730	020427	013616		CMP	R4,#MJR27B		
4044	013734	001403			BEQ	MJR37A		
4045								
4046	013736				2#:			
4047	013736	104000			ERROR			
4048	013740	000330			.WORD	330		
4049	013742	001127			.WORD	CPUERR		
4050								
4051	013744	005237	001066		MJR37A:	INC	0#SEQ	
4052	013750	013706	001070		MOV	0#SPS,R6		
4053	013754	012704	000125		MOV	#125,R4		
4054	013760	004467	177634		JSR	R4,MJR67		

;VERIFY R4 GOT LOADED ON THE STACK
 ;BRANCH IF INCORRECT STACK CONTENTS
 ;VERIFY CORRECT RETURN ADDRESS
 ;BRANCH IF GOOD RETURN ADDRESS ON STACK
 ;ERROR! MODE 27 FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
 ;UNIQUE ERROR NUMBER
 ;ADDRESS OF ERROR MESSAGE

;UPDATE SEQUENCER
 ;SETUP R4 TEST DATA
 ;RESET STACK POINTER
 ;JSR MODE 37

;VERIFY TEST SEQUENCE
 ;INCORRECT TEST SEQUENCE
 ;VERIFY STACK DECREMENT
 ;INCORRECT STACK DECREMENT
 ;VERIFY STACK WAS LOADED

;VERIFY RETURN ADDRESS
 ;BRANCH IF GOOD
 ;ERROR! MODE 67 FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
 ;UNIQUE ERROR NUMBER
 ;ADDRESS OF ERROR MESSAGE

;UPDATE SEQUENCER
 ;RESET STACK
 ;SETUP R4 DATA
 ;JSR MODE 77

;DATA FOR MODE 77 JUMP

;VERIFY TEST SEQUENCE
 ;INCORRECT TEST SEQUENCE
 ;VERIFY STACK DECREMENT
 ;INCORRECT STACK DECREMENT
 ;VERIFY STACK WAS LOADED

;VERIFY RETURN ADDRESS
 ;BRANCH IF GOOD
 ;ERROR! MODE 37 FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
 ;UNIQUE ERROR NUMBER
 ;ADDRESS OF ERROR MESSAGE

;UPDATE SEQUENCER
 ;RELOAD STACK
 ;SETUP R4 TEST DATA
 ;JSR MODE 6

```

4055
4056 013764 023727 001066 000004 MJR77: CMP      @#SEQ,#4      ;VERIFY TEST SEQUENCE
4057 013772 001011                BNE      21          ;INCORRECT TEST SEQUENCE
4058 013774 023706 001072                CMP      @#SPSJ,R6   ;VERIFY STACK DECRIMENT
4059 014000 001006                BNE      21          ;INCORRECT STACK DECRIMENT
4060 014002 021627 000001                CMP      (R6),#1    ;VERIFY STACK WAS LOADED
4061 014006 001003                BNE      21          ;VERIFY RETURN ADDRESS
4062 014010 020427 013700                CMP      R4,@MJR6A  ;BRANCH IF GOOD
4063 014014 001403                BEQ      MJR77A     ;ERROR! MODE 77 FAILED
4064
4065 014016                21:
4066 014016 104000                ERROR
4067 014020 000331                .WORD   331        ;ALL ERRORS TO TRAP TO EMT VECTOR
4068 014022 001127                .WORD   CPUERR     ;UNIQUE ERROR NUMBER
4069
4070 014024                MJR77A:
4071
4072 014024 013706 001070                MOV      @#SPS,R6   ;RESET STACK
4073
4074
4075 014030                ;
4076                ;MRTS:
4077                ;*****
4078                ;*TEST 125      TEST RTS AND RTS R6
4079                ;*****
4080 014030 005267 164750                TST125:
4081 014034 012706 001000                INC      @TESTN     ;INCREMENT TEST NUMBER
4082 014040 012746 123456                MOV      @STBOT,R6  ;INSURE VALID STACK
4083 014044 012703 014060                MOV      @123456,-(R6) ;SETUP TEST REGISTER
4084 014050 000203                MOV      @RTS1,R3   ;SETUP TEST PC
4085 014052 104000                RTS      R3         ;**TEST INSTRUCTION
4086 014054 000332                ERROR
4087 014056 001127                .WORD   332        ;ALL ERRORS TO TRAP TO EMT VECTOR
4088                .WORD   CPUERR     ;UNIQUE ERROR NUMBER
4089                ;INCORRECT PC ON RTS
4090 014060 022703 123456                RTS1:
4091 014064 001403                CMP      @123456,R3
4092                BEQ      RTS6          ;BRANCH IF GOOD
4093 014066 104000                ERROR
4094 014070 000333                .WORD   333        ;ERROR! REGISTER CONTENTS INCORRECT
4095 014072 001127                .WORD   CPUERR     ;ALL ERRORS TO TRAP TO EMT VECTOR
4096                ;UNIQUE ERROR NUMBER
4097                ;ADDRESS OF ERROR MESSAGE
4098
4099                ;THIS TEST CHECKS AN UN-TESTED PLA TERM
4100 014074 010601                RTS6:
4101 014076 012705 014114                MOV      R6,R1      ;SAVE STACK IN R1
4102 014102 010506                MOV      @11,R5     ;MOVE EXPECTED RETURN ADDR TO R5
4103 014104 000206                MOV      R5,R6     ;MOVE RETURN ADDR TO R6
4104                RTS      R6          ;>>>>TEST INSTRUCTION<<<<<
4105 014106 104000                ERROR
4106 014110 000334                .WORD   334        ;ERROR! RTS NOT EXECUTED
4107 014112 001127                .WORD   CPUERR     ;ALL ERRORS TO TRAP TO EMT VECTOR
4108 014114 021506                ;UNIQUE ERROR NUMBER
4109 014116 001403                11:
4110                CMP      (R5),R6  ;ADDRESS OF ERROR MESSAGE
4110                BEQ      RTSE     ;IS R6=31506?
4110                ;IF IT IS THEN GO TO END OF TEST
4110                ;ERROR! WRONG ADDR IN R6

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4111 014120 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4112 014122 000335          .WORD          335          ; UNIQUE ERROR NUMBER
4113 014124 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4114 014126 010106          RTSE: MOV          R1,R6    ; RESTORE STACK
4115
4116 014130          TSMUO:
4117          ;*****
4118          ; TEST 126      SETUP AND TEST KERNEL, SUPERVISOR AND USER STACKS
4119          ;*****
4120 014130          TST126:
4121 014130 005267 164650          INC          $TESTN      ; INCREMENT TEST NUMBER
4122 014134 012737 040000 177776          MOV          $00000,$0177776 ; SET PS TO SUP MODE
4123 014142 012706 177777          MOV          $177777,R6    ; INIT SUP STACK TO ALL ONES
4124 014146 022706 177777          CMP          $177777,R6    ; ARE ALL BITS SET
4125 014152 001403          BEQ          1$          ; YES GO ON
4126          ; NO GO TO ERROR
4127 014154 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4128 014156 000336          .WORD          336          ; UNIQUE ERROR NUMBER
4129 014160 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4130
4131 014162 005006          1$: CLR          R6          ; SET SUP STACK TO ALL ZEROES
4132 014164 022706 000000          CMP          $0,R6        ; ARE ALL BITS CLEARED
4133 014170 001403          BEQ          2$          ; YES GO ON
4134          ; NO GO TO ERROR
4135 014172 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4136 014174 000337          .WORD          337          ; UNIQUE ERROR NUMBER
4137 014176 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4138
4139 014200 012706 125252          2$: MOV          $125252,R6   ; SET SUP STACK TO ALTERNATING PATTERN
4140 014204 022706 125252          CMP          $125252,R6   ; IS SUP SP CORRECT
4141 014210 001403          BEQ          3$          ; YES GO ON
4142          ; NO GO TO ERROR
4143 014212 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4144 014214 000340          .WORD          340          ; UNIQUE ERROR NUMBER
4145 014216 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4146
4147 014220 012706 052525          3$: MOV          $52525,R6   ; SET SUP STACK TO ALTERNATING PATTERN
4148 014224 022706 052525          CMP          $52525,R6   ; IS SUP SP CORRECT
4149 014230 001403          BEQ          4$          ; YES GO ON
4150          ; NO GO TO ERROR
4151 014232 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4152 014234 000341          .WORD          341          ; UNIQUE ERROR NUMBER
4153 014236 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4154
4155 014240 012706 000700          4$: MOV          $700,R6    ; SETUP SUP SP
4156 014244 012737 140000 177776          MOV          $140000,$0177776 ; SET PS TO USER MODE
4157 014252 012706 177777          MOV          $177777,R6    ; INIT USER STACK TO ALL ONES
4158 014256 022706 177777          CMP          $177777,R6    ; ARE ALL BITS SET
4159 014262 001403          BEQ          5$          ; YES GO ON
4160          ; NO GO TO ERROR
4161 014264 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
4162 014266 000342          .WORD          342          ; UNIQUE ERROR NUMBER
4163 014270 001127          .WORD          CPUERR      ; ADDRESS OF ERROR MESSAGE
4164
4165 014272 005006          5$: CLR          R6          ; SET USER STACK TO ALL ZEROES
4166 014274 022706 000000          CMP          $0,R6        ; ARE ALL BITS CLEARED

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4223
4224
4225
4226 014474 012737 040000 177776 CHECK: MOV #40000, @177776 ;SET PSW TO SUP MODE
4227 014502 004767 000060 JSR PC,CHECK1 ; TEST SUP, KER, AND USE STACKS
4228 014506 022716 000000 RET2: CMP #0,(SP) ;IS SUP STACK CLEARED
4229 014512 001403 BEQ 1# ;YES GO ON
4230 ;NO GO TO ERROR
4231 014514 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4232 014516 000351 .WORD 351 ;UNIQUE ERROR NUMBER
4233 014520 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
4234
4235 014522 012737 140000 177776 1#: MOV #140000, @177776 ;SET PSW TO USE MODE
4236 014530 022716 000000 CMP #0,(SP) ;IS USE STACK CLEARED
4237 014534 001403 BEQ 2# ;YES GO ON
4238 ;NO GO TO ERROR
4239 014536 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4240 014540 000352 .WORD 352 ;UNIQUE ERROR NUMBER
4241 014542 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
4242
4243 014544 005037 177776 2#: CLR @177776 ;SET PSW TO KER MODE
4244 014550 022716 014404 CMP @RET1,(SP) ;DOES KER STACK HAVE CORRECT DATA
4245 014554 001403 BEQ 3# ;YES GO ON
4246 ;NO GO TO ERROR
4247 014556 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4248 014560 000353 .WORD 353 ;UNIQUE ERROR NUMBER
4249 014562 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
4250
4251 014564 000207 3#: RTS PC ;RETURN
4252
4253 ;ROUTINE TO CHECK STACKS AFTER ONE RTS
4254
4255 014566 012737 140000 177776 CHECK1: MOV #140000, @177776 ;SET PSW TO USE MODE
4256 014574 004767 000060 JSR PC,CHECK2 ; TEST KER, SUP, AND USE STACKS
4257 014600 022716 000000 RET3: CMP #0,(SP) ;IS USE STACK CLEARED
4258 014604 001403 BEQ 1# ;YES GO ON
4259 ;NO GO TO ERROR
4260 014606 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4261 014610 000354 .WORD 354 ;UNIQUE ERROR NUMBER
4262 014612 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
4263
4264 014614 005037 177776 1#: CLR @177776 ;SET PSW TO KER MODE
4265 014620 022716 014404 CMP @RET1,(SP) ;IS KER STACK CORRECT
4266 014624 001403 BEQ 2# ;YES GO ON
4267 ;NO GO TO ERROR
4268 014626 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4269 014630 000355 .WORD 355 ;UNIQUE ERROR NUMBER
4270 014632 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
4271
4272 014634 012737 040000 177776 2#: MOV #40000, @177776 ;SET PSW TO SUP MODE
4273 014642 022716 014506 CMP @RET2,(SP) ;IS SUP STACK CORRECT
4274 014646 001403 BEQ 3# ;YES GO ON
4275 ;NO GO TO ERROR
4276 014650 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
4277 014652 000356 .WORD 356 ;UNIQUE ERROR NUMBER
4278 014654 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE

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4279
4280 014656 000207      3#:   RTS      PC           ;RETURN
4281
4282                    ;ROUTINE TO CHECK STACKS AFTER ZERO RTS
4283
4284 014660 022716 014600  CHECK2: CMP      @RET3,(SP)    ;IS USE STACK CORRECT
4285 014664 001403                BEQ      1#                 ;YES GO ON
4286                                ;NO GO TO ERROR
4287 014666 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
4288 014670 000357                .WORD    357                ;UNIQUE ERROR NUMBER
4289 014672 001127                .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
4290
4291 014674 012737 040000 177776 1#:   MOV      @40000,@#177776    ;SET PSW TO SUP MODE
4292 014702 022716 014506                CMP      @RET2,(SP)        ;IS SUP STACK CORRECT
4293 014706 001403                BEQ      2#                 ;YES GO ON
4294                                ;NO GO TO ERROR
4295 014710 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
4296 014712 000360                .WORD    360                ;UNIQUE ERROR NUMBER
4297 014714 001127                .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
4298
4299 014716 005037 177776 2#:   CLR      @#177776          ;SET PSW TO KER MODE
4300 014722 022716 014404                CMP      @RET1,(SP)        ;IS KER STACK CORRECT
4301 014726 001403                BEQ      3#                 ;YES GO ON
4302                                ;NO GO TO ERROR
4303 014730 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
4304 014732 000361                .WORD    361                ;UNIQUE ERROR NUMBER
4305 014734 001127                .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
4306
4307 014736 012737 140000 177776 3#:   MOV      @140000,@#177776    ;SET PSW TO USE MODE
4308 014744 000207                RTS      PC                 ;RETURN
4309
4310 014746                    ; MTSO:
4311 014746                    ; MMVCC:
4312
4313                    ;*****
4314                    ;*TEST 127      TEST MOV CONDITION CODES - **0-
4315                    ;*****
4316 014746 005267 164032  TST127: INC      @TESTN          ;INCREMENT TEST NUMBER
4317 014752 000277                SCC
4318 014754 000244                CLZ
4319 014756 012704 000000                MOV      @0,R4             ;CC=1011
4320 014762 100403                BMI      1#                 ;CC=0101, R4=0
4321 014764 102402                BVS      1#                 ;ERROR IF N FLAG
4322 014766 103001                BCC      1#                 ;ERROR IF V FLAG SET
4323 014770 001403                BEQ      2#                 ;ERROR IF C FLAG CLEAR
4324                                ;SKIP IF Z FLAG SET
4325                                ;CC SHOULD=0101
4326 014772 104000                ERROR                ;ALL ERRORS TO TRAP TO EMT VECTOR
4327 014774 000362                .WORD    362                ;UNIQUE ERROR NUMBER
4328 014776 001127                .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
4329
4330 015000 000277                2#:   SCC
4331 015002 000251                .WORD    251                ;CC=0110
4332 015004 012704 100000                MOV      @100000,R4        ;R4=100000, CC=1000
4333 015010 001403                BEQ      3#                 ;ERROR IF Z SET
4334 015012 102402                BVS      3#                 ;ERROR IF V SET

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4335 015014 103401          BCS      3#
4336 015016 100403          BMI      4#
4337
4338 015020          3#:
4339 015020 104000          ERROR
4340 015022 000363          .WORD   363
4341 015024 001127          .WORD   CPUERR
4342
4343 015026          4#:
4344
4345
4346 015026          MBTCC:
4347          ;*****
4348          ;*TEST 130      TEST BIT CONDITION CODES - **0-
4349          ;*****
4350 015026          TST130:
4351 015026 005267 163752          INC      #TESTN          ;INCREMENT TEST NUMBER
4352 015032 005004          CLR      R4
4353 015034 005104          COM      R4          ;R4=-1
4354 015036 000277          SCC
4355 015040 000244          CLZ          ;
4356 015042 032704 000000          BIT      #0,R4          ;CC=1011
4357 015046 100403          BMI      1#          ;CC=0101
4358 015050 102402          BVS      1#          ;ERROR IF N FLAG
4359 015052 103001          BCC      1#          ;ERROR IF V FLAG SET
4360 015054 001403          BEQ      2#          ;ERROR IF C FLAG CLEAR
4361
4362 015056          1#:
4363 015056 104000          ERROR
4364 015060 000364          .WORD   364
4365 015062 001127          .WORD   CPUERR
4366
4367 015064 000277          2#:
4368 015066 000251          SCC
4369 015070 032704 100000          .WORD   251
4370 015074 001403          BIT      #100000,R4
4371 015076 102402          BEQ      3#
4372 015100 103401          BVS      3#
4373 015102 100403          BCS      3#
4374          BMI      4#
4375 015104          3#:
4376 015104 104000          ERROR
4377 015106 000365          .WORD   365
4378 015110 001127          .WORD   CPUERR
4379
4380 015112          4#:
4381
4382
4383 015112          MBCCC:
4384          ;*****
4385          ;*TEST 131      TEST BIC CONDITION CODES - **0-
4386          ;*****
4387 015112          TST131:
4388 015112 005267 163666          INC      #TESTN          ;INCREMENT TEST NUMBER
4389 015116 005004          CLR      R4
4390 015120 005104          COM      R4          ;R4=-1

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4391 015122 000277          SCC
4392 015124 000244          CLZ
4393 015126 042704 177777  BIC      #177777,R4
4394 015132 100403          BMI      1#
4395 015134 102402          BVS      1#
4396 015136 103001          BCC      1#
4397 015140 001403          BEQ      2#
4398
4399 015142          1#:
4400 015142 104000          ERROR
4401 015144 000366          .WORD   366
4402 015146 001127          .WORD   CPUERR
4403
4404 015150 005104          2#:  COM      R4
4405 015152 000277          SCC
4406 015154 000251          .WORD   251
4407 015156 042704 077777  BIC      #77777,R4
4408 015162 001403          BEQ      3#
4409 015164 102402          BVS      3#
4410 015166 103401          BCS      3#
4411 015170 100403          BMI      4#
4412
4413 015172          3#:
4414 015172 104000          ERROR
4415 015174 000367          .WORD   367
4416 015176 001127          .WORD   CPUERR
4417
4418 015200          4#:
4419
4420
4421 015200
4422
4423
4424
4425 015200
4426 015200 005267 163600
4427 015204 005004
4428 015206 000277
4429 015210 000246
4430 015212 052704 000000  BIS      #0,R4
4431 015216 100403          BMI      1#
4432 015220 102402          BVS      1#
4433 015222 103001          BCC      1#
4434 015224 001403          BEQ      2#
4435
4436 015226          1#:
4437 015226 104000          ERROR
4438 015230 000370          .WORD   370
4439 015232 001127          .WORD   CPUERR
4440
4441 015234 000277          2#:  SCC
4442 015236 000241          CLC
4443 015240 052704 100076  BIS      #100076,R4
4444 015244 001403          BEQ      3#
4445 015246 102402          BVS      3#
4446 015250 103401          BCS      3#

;
;CC=1011
;CC=0101
;ERROR IF N FLAG
;ERROR IF V FLAG SET
;ERROR IF C FLAG CLEAR
;SKIP IF Z FLAG SET
;ERROR! CC SHOULD=0101

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;R4=-1

;CC=0110
;CC=1000
;ERROR IF Z SET
;ERROR IF V SET
;ERROR IF C SET
;EXIT IF N SET
;ERROR! CC SHOULD= 1000

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;INCREMENT TEST NUMBER
;R4=0

;CC=1001
;R4=0, CC=0101
;ERROR IF MINUS
;ERROR IF V SET
;ERROR IF C CLEAR
;BRANCH IF GOOD
;ERROR! BIS CC FAILED

;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

;CC=1110
;R4=100076, CC=1000
;ERROR IF Z SET
;ERROR IF V SET
;ERROR IF C SET

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4447 015252 100403          BMI      4#          ;BRANCH IF GOOD
4448                                     ;ERROR! BAD BIS CC
4449 015254          3#:
4450 015254 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
4451 015256 000371          .WORD      371          ;UNIQUE ERROR NUMBER
4452 015260 001127          .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
4453
4454 015262          4#:
4455
4456
4457 015262          MDCCC:
4458          ;*****
4459          ;*TEST 133      TEST DEC, INC CONDITION CODES
4460          ;*****
4461 015262          TST133:
4462 015262 005267 163516    INC      #TESTN          ;INCREMENT TEST NUMBER
4463 015266 012704 077777    MOV      #77777,R4      ;R4=77777
4464 015272 000257          CCC
4465 015274 000261          SEC          ;CC=0001
4466 015276 005204          INC      R4          ;R4=100000, CC=0011
4467 015300 001403          BEQ      1#          ;ERROR IF ZERO
4468 015302 100002          BPL      1#          ;ERROR IF POSITIVE
4469 015304 102001          BVC      1#          ;ERROR IF V CLEAR
4470 015306 103403          BCS      2#          ;BRANCH IF GOOD
4471                                     ;ERROR! INC FAILED
4472 015310          1#:
4473 015310 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
4474 015312 000372          .WORD      372          ;UNIQUE ERROR NUMBER
4475 015314 001127          .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
4476
4477 015316 000257          2#:  CCC
4478 015320 005204          INC      R4          ;R4=100001, CC=1000
4479 015322 103413          BCS      3#          ;ERROR IF C SET
4480 015324 102412          BVS      3#          ;ERROR IF V SET
4481 015326 005304          DEC      R4          ;R4=100000, CC=1000
4482 015330 102410          BVS      3#          ;ERROR IF V SET
4483 015332 103407          BCS      3#          ;ERROR IF C SET
4484 015334 000277          SCC
4485 015336 000252          .WORD      252          ;
4486 015340 005304          DEC      R4          ;CC=0101
4487 015342 001403          BEQ      3#          ;R4=77777, CC=1011
4488 015344 102002          BVC      3#          ;ERROR IF Z SET
4489 015346 103001          BCC      3#          ;ERROR IF V CLEAR
4490 015350 100003          BPL      4#          ;ERROR IF C CLEAR
4491                                     ;BRANCH IF GOOD
4492 015352          3#:          ;ERROR! BAD CC
4493 015352 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
4494 015354 000373          .WORD      373          ;UNIQUE ERROR NUMBER
4495 015356 001127          .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
4496
4497 015360          4#:
4498
4499
4500 015360          MCTSCC:
4501          ;*****
4502          ;*TEST 134      TEST CLR, TST, SWAB CONDITION CODES

```

```

4503
4504
4505
4506 015360
4507 015360 005267 163420
4508 015364 000277
4509 015366 000244
4510 015370 005004
4511 015372 100403
4512 015374 102402
4513 015376 103401
4514 015400 001403
4515
4516 015402
4517 015402 104000
4518 015404 000374
4519 015406 001127
4520
4521 015410 005104
4522 015412 000277
4523 015414 005704
4524 015416 001403
4525 015420 102402
4526 015422 103401
4527 015424 100403
4528
4529 015426
4530 015426 104000
4531 015430 000375
4532 015432 001127
4533
4534 015434 000277
4535 015436 000304
4536 015440 102402
4537 015442 103401
4538 015444 100403
4539
4540 015446
4541 015446 104000
4542 015450 000376
4543 015452 001127
4544
4545 015454
4546
4547
4548 015454
4549
4550
4551
4552 015454
4553 015454 005267 163324
4554 015460 012704 077777
4555 015464 012701 000001
4556 015470 000257
4557 015472 060401
4558 015474 102003

```

```

;*****
;0100 - **00 - **00
;*****
TST134:
      INC      #TESTN          ;INCREMENT TEST NUMBER
      SCC
      CLZ
      CLR      R4              ;CC=1011
      BMI     1#              ;R4=0, CC=0100
      BVC     1#              ;ERROR IF MINUS
      BCS     1#              ;ERROR IF V SET
      BEQ     2#              ;ERROR IF C SET
      BEQ     2#              ;BRANCH IF GOOD
      BEQ     2#              ;ERROR! BAD CC ON CLR
1#:
      ERROR   .WORD 374       ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   .WORD CPUERR   ;UNIQUE ERROR NUMBER
      .WORD   .WORD CPUERR   ;ADDRESS OF ERROR MESSAGE
2#:
      COM     R4              ;R4=-1
      SCC
      TST     R4              ;CC=1111
      BEQ     3#              ;CC=1000
      BVS     3#              ;ERROR IF Z SET
      BVS     3#              ;ERROR IF V SET
      BCS     3#              ;ERROR IF C SET
      BMI     4#              ;BRANCH IF GOOD
      BMI     4#              ;ERROR! BAD TST CC
3#:
      ERROR   .WORD 375       ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   .WORD CPUERR   ;UNIQUE ERROR NUMBER
      .WORD   .WORD CPUERR   ;ADDRESS OF ERROR MESSAGE
4#:
      SCC
      SWAB    R4              ;CC=1111
      BVS     5#              ;CC=1000
      BCS     5#              ;ERROR IF V SET
      BMI     6#              ;ERROR IF C SET
      BMI     6#              ;BRANCH IF GOOD
      BMI     6#              ;ERROR! BAD SWAB CC
5#:
      ERROR   .WORD 376       ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   .WORD CPUERR   ;UNIQUE ERROR NUMBER
      .WORD   .WORD CPUERR   ;ADDRESS OF ERROR MESSAGE
6#:
MADCC:
;*****
;#TEST 135      TEST ADD CONDITION CODES - ****
;*****
TST135:
      INC      #TESTN          ;INCREMENT TEST NUMBER
      MOV     #77777,R4       ;R4=77777
      MOV     #1,R1          ;R1=1
      CCC
      ADD     R4,R1           ;CC=0000
      BVC     1#              ;77777 * 1 = 100000 IN R1
      BVC     1#              ;ERROR IF V CLEAR

```



```

4671 015730 012704 077777      4:  MOV      #77777,R4      ;R4=77777
4672 015734 012701 170000      MOV      #170000,R1     ;R1=170000
4673 015740 000257                CCC                    ;CC=0000
4674 015742 020401                CMP      R4,R1         ;77777 - 170000 = 107777 CC= 1011
4675 015744 102003                BVC     5:             ;ERROR IF V CLEAR
4676 015746 103002                BCC     5:             ;ERROR IF C CLEAR
4677 015750 001401                BEQ     5:             ;ERROR IF ZERO
4678 015752 100403                BMI     6:             ;BRANCH IF GOOD
4679                                ;ERROR! BAD CMP
4680 015754                        5:
4681 015754 104000                ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
4682 015756 000407                .WORD   407                ;UNIQUE ERROR NUMBER
4683 015760 001127                .WORD   CPUERR            ;ADDRESS OF ERROR MESSAGE
4684
4685 015762 000257                6:  CCC                    ;R1=7777
4686 015764 005101                COM      R1                ;ERROR IF MINUS
4687 015766 100403                BMI     7:             ;ERROR IF ZERO
4688 015770 001402                BEQ     7:             ;ERROR IF CARRY
4689 015772 103001                BCC     7:             ;ERROR IF ZERO
4690 015774 102003                BVC     8:             ;BRANCH IF GOOD
4691                                ;ERROR! BAD COM
4692 015776                        7:
4693 015776 104000                ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
4694 016000 000410                .WORD   410                ;UNIQUE ERROR NUMBER
4695 016002 001127                .WORD   CPUERR            ;ADDRESS OF ERROR MESSAGE
4696
4697 016004 000277                8:  SCC                    ;R1=7777
4698 016006 005101                COM      R1                ;ERROR IF MINUS
4699 016010 100403                BMI     10:            ;ERROR IF ZERO
4700                                ;ERROR! BAD COM
4701 016012                        9:
4702 016012 104000                ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
4703 016014 000411                .WORD   411                ;UNIQUE ERROR NUMBER
4704 016016 001127                .WORD   CPUERR            ;ADDRESS OF ERROR MESSAGE
4705
4706 016020                        10:
4707
4708
4709 016020                MSBCC:
4710                ;*****
4711                ;*TEST 140      TEST SUB CONDITION CODES - ****
4712                ;*****
4713 016020                TST140:
4714 016020 005267 162760                INC      #TESTN           ;INCREMENT TEST NUMBER
4715 016024 012704 077775                MOV      #77775,R4       ;R4=77775
4716 016030 000257                CCC                    ;CC=0000
4717 016032 162704 137757                SUB      #137757,R4      ;77775 - 137757
4718                                ;TRY TO CAUSE AN ARITHMETIC OVERFLOW
4719 016036 102003                BVC     1:             ;ERROR IF V CLEAR
4720 016040 100002                BPL     1:             ;ERROR IF RESULT IS POSITIVE
4721 016042 001401                BEQ     1:             ;ERROR IF Z SET
4722 016044 103403                BCS     2:             ;BRANCH IF GOOD
4723                                ;ERROR! BAD SUBTRACT
4724 016046                        1:
4725 016046 104000                ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
4726 016050 000412                .WORD   412                ;UNIQUE ERROR NUMBER

```


Address	Area	Code	Condition	Register	Description
4783	016200	000415	.WORD	415	:UNIQUE ERROR NUMBER
4784	016202	001127	.WORD	CPUERR	:ADDRESS OF ERROR MESSAGE
4785					
4786	016204				
4787					
4788					
4789	016204				
4790					
4791					
4792					
4793	016204				
4794	016204	005267	INC	%TESTN	:INCREMENT TEST NUMBER
4795	016210	012704	MOV	%60000,R4	:R4= 0110000000000000
4796	016214	000257	CCC		:CC=0000
4797	016216	006104	ROL	R4	:R4= 1100000000000000
4798	016220	103402	BCS	1%	:ERROR IF CARRY
4799	016222	102001	BVC	1%	:ERROR IF V CLEAR
4800	016224	100403	BMI	2%	:BRANCH IF GOOD
4801					:ERROR! ROL FAILED
4802	016226				
4803	016226	104000	ERROR		:ALL ERRORS TO TRAP TO EMT VECTOR
4804	016230	000416	.WORD	416	:UNIQUE ERROR NUMBER
4805	016232	001127	.WORD	CPUERR	:ADDRESS OF ERROR MESSAGE
4806					
4807	016234	006104	ROL	R4	:R4= 1000000000000000
4808	016236	103002	BCC	3%	:ERROR IF CARRY CLEAR
4809	016240	102401	BVS	3%	:ERROR IF V SET
4810	016242	100403	BMI	4%	:BRANCH IF GOOD
4811					:ERROR! BAD ROL
4812	016244				
4813	016244	104000	ERROR		:ALL ERRORS TO TRAP TO EMT VECTOR
4814	016246	000417	.WORD	417	:UNIQUE ERROR NUMBER
4815	016250	001127	.WORD	CPUERR	:ADDRESS OF ERROR MESSAGE
4816					
4817	016252	006104	ROL	R4	:R4 = 0000000000000001
4818	016254	102003	BVC	5%	:ERROR IF V CLEAR
4819	016256	103002	BCC	5%	:ERROR IF C CLEAR
4820	016260	100401	BMI	5%	:ERROR IF MINUS
4821	016262	001003	BNE	6%	:BRANCH IF GOOD
4822					:ERROR! BAD ROL
4823	016264				
4824	016264	104000	ERROR		:ALL ERRORS TO TRAP TO EMT VECTOR
4825	016266	000420	.WORD	420	:UNIQUE ERROR NUMBER
4826	016270	001127	.WORD	CPUERR	:ADDRESS OF ERROR MESSAGE
4827					
4828	016272	006104	ROL	R4	:R4=0000000000000011
4829	016274	102402	BVS	7%	:ERROR IF V SET
4830	016276	103401	BCS	7%	:ERROR IF C SET
4831	016300	100003	BPL	8%	:BRANCH IF GOOD
4832					:ERROR! BAD ROL
4833	016302				
4834	016302	104000	ERROR		:ALL ERRORS TO TRAP TO EMT VECTOR
4835	016304	000421	.WORD	421	:UNIQUE ERROR NUMBER
4836	016306	001127	.WORD	CPUERR	:ADDRESS OF ERROR MESSAGE
4837					
4838	016310				

4839
4840
4841 016310
4842
4843
4844
4845 016310
4846 016310 005267 162470
4847 016314 012704 000003
4848 016320 000257
4849 016322 006004
4850 016324 103002
4851 016326 102001
4852 016330 100003
4853
4854 016332
4855 016332 104000
4856 016334 000422
4857 016336 001127
4858
4859 016340 006004
4860 016342 103002
4861 016344 102401
4862 016346 100403
4863
4864 016350
4865 016350 104000
4866 016352 000423
4867 016354 001127
4868
4869 016356 006004
4870 016360 102002
4871 016362 103401
4872 016364 100403
4873
4874 016366
4875 016366 104000
4876 016370 000424
4877 016372 001127
4878
4879 016374 006004
4880 016376 102402
4881 016400 103401
4882 016402 100003
4883
4884 016404
4885 016404 104000
4886 016406 000425
4887 016410 001127
4888
4889 016412
4890
4891
4892
4893
4894

MRRCC:

```

;*****
;TEST 143 TEST ROR CONDITION CODES - *****
;*****
TST143:

```

```

      INC      #TESTN      ;INCREMENT TEST NUMBER
      MOV      #3,R4      ;R4= 0000000000000011
      CCC      ;CC= 0000
      ROR      R4          ;R4= 0000000000000001
      BCC      1#        ;ERROR IF NO CARRY
      BVC      1#        ;ERROR IF V CLEAR
      BPL      2#        ;BRANCH IF GOOD
                        ;ERROR! ROR FAILED

1#:
      ERROR
      .WORD   422
      .WORD   CPUERR
                        ;ALL ERRORS TO TRAP TO EMT VECTOR
                        ;UNIQUE ERROR NUMBER
                        ;ADDRESS OF ERROR MESSAGE

2#:
      ROR      R4          ;R4= 1000000000000000
      BCC      3#        ;ERROR IF CARRY CLEAR
      BVS      3#        ;ERROR IF V SET
      BMI      4#        ;BRANCH IF GOOD
                        ;ERROR! BAD ROR

3#:
      ERROR
      .WORD   423
      .WORD   CPUERR
                        ;ALL ERRORS TO TRAP TO EMT VECTOR
                        ;UNIQUE ERROR NUMBER
                        ;ADDRESS OF ERROR MESSAGE

4#:
      ROR      R4          ;R4 = 1100000000000000
      BVC      5#        ;ERROR IF V
      BCS      5#        ;ERROR IF C SET
      BMI      6#        ;BRANCH IF GOOD
                        ;ERROR! BAD ROR

5#:
      ERROR
      .WORD   424
      .WORD   CPUERR
                        ;ALL ERRORS TO TRAP TO EMT VECTOR
                        ;UNIQUE ERROR NUMBER
                        ;ADDRESS OF ERROR MESSAGE

6#:
      ROR      R4          ;R4= 0110000000000000
      BVS      7#        ;ERROR IF V SET
      BCS      7#        ;ERROR IF C SET
      BPL      8#        ;BRANCH IF GOOD
                        ;ERROR! BAD ROR

7#:
      ERROR
      .WORD   425
      .WORD   CPUERR
                        ;ALL ERRORS TO TRAP TO EMT VECTOR
                        ;UNIQUE ERROR NUMBER
                        ;ADDRESS OF ERROR MESSAGE

8#:
;*****
;TEST 144 TEST C BIT WITH ROR/ROL

```



```

4895
4896
4897
4898
4899 016412
4900 016412 005267 162366
4901 016416 012701 052525
4902 016422 000241
4903 016424 006001
4904 016426 006001
4905 016430 006001
4906 016432 103403
4907 016434 104000
4908 016436 000426
4909 016440 001127
4910 016442 022701 045252
4911 016446 001403
4912 016450 104000
4913 016452 000427
4914 016454 001127
4915 016456 012701 125252
4916 016462 000241
4917 016464 006101
4918 016466 006101
4919 016470 006101
4920 016472 103403
4921 016474 104000
4922 016476 000430
4923 016500 001127
4924 016502 022701 052522
4925 016506 001403
4926 016510 104000
4927 016512 000431
4928 016514 001127
4929 016516
4930
4931
4932 016516
4933
4934
4935
4936 016516
4937 016516 005267 162262
4938 016522 012704 060000
4939 016526 000257
4940 016530 006304
4941 016532 103402
4942 016534 102001
4943 016536 100403
4944
4945 016540
4946 016540 104000
4947 016542 000432
4948 016544 001127
4949
4950 016546 006304

```

```

;*****
;THIS TEST IS TO CHECK FOR A SLOW C BIT PATH INTERNAL TO THE J11 DATA CHIP
;PROBLEM IS ONLY EXHIBITED ON EARLY MASK SETS (1590 AND 1593)
;*****
TST144:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      MOV      $52525,R1      ;INIT R1 WITH DATA
      CLC
      ROR      R1             ;CLEAR THE C BIT
      ROR      R1             ;R1=025252, C BIT =1
      ROR      R1             ;R1=112525, C BIT =0
      ROR      R1             ;R1=045252, C BIT =1
      BCS      1$            ;BRANCH IF CARRY BIT SET
      ERROR    426           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR        ;UNIQUE ERROR NUMBER
      .WORD    045252,R1     ;ADDRESS OF ERROR MESSAGE
1$:   CMP      $45252,R1     ;IS DATA IN R1 = TO EXPECTED DATA?
      BEQ      2$            ;BRANCH IF YES
      ERROR    427           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR        ;UNIQUE ERROR NUMBER
      .WORD    045252,R1     ;ADDRESS OF ERROR MESSAGE
2$:   MOV      $125252,R1    ;SET UP R1
      CLC
      ROL      R1             ;CLEAR THE CARRY BIT
      ROL      R1             ;R1=052524, C BIT =1
      ROL      R1             ;R1=125251, C BIT =0
      ROL      R1             ;R1=052522, C BIT =1
      BCS      3$            ;BRANCH IF CARRY SET
      ERROR    430           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR        ;UNIQUE ERROR NUMBER
      .WORD    052522, R1    ;ADDRESS OF ERROR MESSAGE
3$:   CMP      $052522, R1   ;IS DATA IN R1 = TO EXPECTED DATA?
      BEQ      4$            ;BRANCH IF YES
      ERROR    431           ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    CPUERR        ;UNIQUE ERROR NUMBER
      .WORD    052522, R1    ;ADDRESS OF ERROR MESSAGE
4$:

```

```

MALCC:
;*****
;*TEST 145      TEST ASL CONDITION CODES - ****
;*****
TST145:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      MOV      $60000,R4      ;R4= 0110000000000000
      CCC
      ASL      R4             ;CC=0000
      BCS      1$            ;C=0 R4= 1100000000000000
      BVC      1$            ;ERROR IF CARRY
      BMI      2$            ;ERROR IF V CLEAR
      BNC      2$            ;BRANCH IF GOOD
1$:   ERROR    432           ;ERROR! ASL FAILED
      .WORD    CPUERR        ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD    432           ;UNIQUE ERROR NUMBER
      .WORD    CPUERR        ;ADDRESS OF ERROR MESSAGE
2$:   ASL      R4             ;C=1 R4= 1000000000000000

```



```

5007
5008 016666          3#:
5009 016666 104000   ERROR
5010 016670 000437   .WORD 437
5011 016672 001127   .WORD CPUERR
5012
5013 016674 006204   4#: ASR R4
5014 016676 102002   BVC 5#
5015 016700 103401   BCS 5#
5016 016702 100403   BMI 6#
5017
5018 016704          5#:
5019 016704 104000   ERROR
5020 016706 000440   .WORD 440
5021 016710 001127   .WORD CPUERR
5022
5023 016712 006204   6#: ASR R4
5024 016714 102005   BVC 7#
5025 016716 103404   BCS 7#
5026 016720 100003   BPL 7#
5027 016722 022704 170016 CMP #170016,R4
5028 016726 001403   BEQ 8#
5029
5030 016730          7#:
5031 016730 104000   ERROR
5032 016732 000441   .WORD 441
5033 016734 001127   .WORD CPUERR
5034
5035 016736          8#:
5036
5037
5038 016736          MSXTCC:
5039 ;*****
5040 ;*TEST 147 TEST SXT CONDITION CODES / -*0-
5041 ;*****
5042 016736          TST147:
5043 016736 005267 162042 INC #TESTN ;INCREMENT TEST NUMBER
5044 016742 012704 123456 MOV #123456,R4 ;SAVE CONTENTS
5045 016746 010401 MOV R4,R1 ;R4=123456
5046 016750 000257 CCC ;SAVE CONTENTS
5047 016752 006704 SXT R4 ;CC=0000
5048 016754 103403 BCS 1# ;R4=0 CC=0100
5049 016756 100402 BMI 1# ;ERROR IF CARRY
5050 016760 102401 BVS 1# ;ERROR IF MINUS
5051 016762 001403 BEQ 2# ;ERROR IF OVERFLOW
5052
5053 016764          1#:
5054 016764 104000   ERROR
5055 016766 000442   .WORD 442
5056 016770 001127   .WORD CPUERR
5057
5058 016772 010104   2#: MOV #1,R4 ;RESTORE R4
5059 016774 000277   SCC ;CC=1111
5060 016776 006704   SXT R4 ;R4=-1 CC=1001
5061 017000 001405   BEQ 3# ;ERROR IF ZERO
5062 017002 100004   BPL 3# ;ERROR IF PLUS

```

5063	017004	103003		BCC	3#		;ERROR IF NO CARRY
5064	017006	102402		BVS	3#		;ERROR IF OVERFLOW
5065	017010	005104		COM	R4		;R4=0
5066	017012	001403		BEQ	4#		;BRANCH IF GOOD
5067							;ERROR! BAD SXT
5068	017014						
5069	017014	104000	3#:	ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5070	017016	000443		.WORD	443		;UNIQUE ERROR NUMBER
5071	017020	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5072							
5073	017022		4#:				
5074							
5075							
5076	017022						
5077							
5078							
5079							
5080	017022						
5081	017022	005267	161756	INC	#TESTN		;INCREMENT TEST NUMBER
5082	017026	012704	123456	MOV	#123456,R4		;R4=123456
5083	017032	012701	052525	MOV	#52525,R1		;R1=52525
5084	017036	000257		CCC			;CC=0000
5085	017040	074104		XOR	R1,R4		;#TI# R4=171173
5086	017042	102403		BVS	1#		;ERROR IF OVERFLOW
5087	017044	001402		BEQ	1#		;ERROR IF ZERO
5088	017046	103401		BCS	1#		;ERROR IF CARRY
5089	017050	100403		BMI	2#		;BRANCH IF GOOD
5090							;ERROR! BAD XOR
5091	017052						
5092	017052	104000	1#:	ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5093	017054	000444		.WORD	444		;UNIQUE ERROR NUMBER
5094	017056	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5095							
5096	017060	012701	125252	MOV	#125252,R1		;R1=125252
5097	017064	000277		SCC			;CC=1111
5098	017066	074104		XOR	R1,R4		;R4=054321
5099	017070	100403		BMI	3#		;ERROR IF MINUS
5100	017072	001402		BEQ	3#		;ERROR IF ZERO
5101	017074	103001		BCC	3#		;ERROR IF CARRY CLEAR
5102	017076	102003		BVC	4#		;BRANCH IF GOOD
5103							;ERROR! BAD XOR
5104	017100						
5105	017100	104000	3#:	ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5106	017102	000445		.WORD	445		;UNIQUE ERROR NUMBER
5107	017104	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5108							
5109	017106	074404					
5110	017110	102406	4#:	XOR	R4,R4		;R4=0
5111	017112	100405		BVS	5#		;ERROR IF OVREFLOW
5112	017114	103004		BMI	5#		;ERROR IF MINUS
5113	017116	001003		BCC	5#		;ERROR IF NO CARRY
5114	017120	022704	000000	BNE	5#		;ERROR IF NOT ZERO
5115	017124	001403		CMP	#0,R4		;SEE IF EXPECTED RESULT
5116				BEQ	6#		;BRANCH IF GOOD
5117	017126						;ERROR! BAD XOR
5118	017126	104000	5#:	ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR

```

MXRCC:
;*****
;#TEST 150      TEST XOR CONDITION CODES / ##0-
;*****
TST150:

```



```

5119 017130 000446          .WORD 446          ;UNIQUE ERROR NUMBER
5120 017132 001127          .WORD CPUERR       ;ADDRESS OF ERROR MESSAGE
5121
5122 017134                6#:
5123
5124
5125
5126 017134                ;
5127                      ;MSXT:
5128                      ;*****
5129                      ;*TEST 151      TEST SXT (SIGN EXTEND INSTRUCTION)
5130                      ;*****
5131                      ;AN ADDITIONAL TEST IS INCLUDED TO CHECK FOR A SLOW N BIT PATH
5132                      ;ON A TRANSITION FROM ZERO TO ONE INTERNAL TO THE J11 DATA CHIP
5133                      ;THE PROBLEM IS ONLY EXHIBITED ON EARLY MASK SETS (1590 OR 1593)
5134                      ;*****
5135 017134 005267 161644    TST151:
5136 017140 005004          INC      #TESTN      ;INCREMENT TEST NUMBER
5137 017142 000257          CLR      R4          ;TRASH R4
5138 017144 000271          CCC          ;CC=0000
5139 017146 006704          .WORD 271          ;CC=1001
5140 017150 102405          SXT      R4          ;*TEST INSTRUCTION
5141 017152 100004          BVS     1#          ;BRANCH IF OVERFLOW IS NOT CLEARED
5142 017154 001403          BPL     1#          ;BRANCH IF N BIT EFFECTED
5143 017156 103002          BEQ     1#          ;BRANCH IF Z BIT EFFECTED
5144 017160 005204          BCC     1#          ;BRANCH IF C BIT EFFECTED
5145 017162 001403          INC      R4          ;BRANCH IF R4 =0
5146                      BEQ     2#          ;ERROR! CC SHOULD HAVE = 1101
5147 017164
5148 017164 104000          1#:
5149 017166 000447          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5150 017170 001127          .WORD 447          ;UNIQUE ERROR NUMBER
5151 017172 000277          .WORD CPUERR       ;ADDRESS OF ERROR MESSAGE
5152 017174 000250          2#:
5153 017176 005004          SCC          ;CC=0111
5154 017200 012714 000055    CLR      R4          ;TRASH R4
5155 017204 006714          MOV     #55,(R4)    ;*TEST INSTRUCTION
5156 017206 001005          SXT     (R4)        ;BRANCH IF BIT EFFECTED
5157 017210 102404          BNE     3#          ;BRANCH IF OVERFLOW
5158 017212 103403          BVS     3#          ;
5159 017214 100402          BCS     3#          ;BRANCH IF N IS SET
5160 017216 005714          BMI     3#          ;VERIFY INSTRUCTION WORKED
5161 017220 001403          TST     (R4)        ;BRANCH IF R4=0
5162                      BEQ     4#          ;ERROR! SXT FAILED
5163 017222          3#:
5164 017222 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5165 017224 000450          .WORD 450          ;UNIQUE ERROR NUMBER
5166 017226 001127          .WORD CPUERR       ;ADDRESS OF ERROR MESSAGE
5167
5168                      ;
5169                      ;NOW TEST FOR SLOW N BIT IN J11 DATA CHIP
5170 017230 012700 177777    4#:
5171 017234 005004          MOV     #-1,R0      ;R0=177777, N BIT = 1
5172 017236 006700          CLR     R4          ;CLEAT THE N BIT
5173                      SXT     R0          ;****TEST INSTRUCTION***
5174 017240 005700          TST     R0          ;TEST N BIT TRANSITION 1 TO 0
                      ;R0 SHOULD = 0

```



```

5343
5344 ;*****
5345 ;*TEST 155 TEST CCC (CLEAR CONDITION CODES) INSTRUCTION
5346 ;*****
5346 017672 TST155:
5347 017672 005267 161106 INC #TESTN ;INCREMENT TEST NUMBER
5348 017676 012737 030017 177776 MOV #30017,0#177776 ;SETUP PSW
5349 017704 000257 CCC ;TEST INSTRUCTION
5350 017706 022737 030000 177776 CMP #30000,0#177776 ;DID IT CLEAR ALL CONDITION CODE BITS
5351 017714 001403 BEQ 1# ;YES GO ON
5352 ;NO GO TO ERROR
5353 017716 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
5354 017720 000470 .WORD 470 ;UNIQUE ERROR NUMBER
5355 017722 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
5356 017724 1#
5357
5358
5359
5360 ;*****
5361 ;*TEST 156 TEST CLEAR C BIT INSTRUCTION
5362 ;*****
5363 017724 TST156:
5364 017724 005267 161054 INC #TESTN ;INCREMENT TEST NUMBER
5365 017730 012737 030017 177776 MOV #30017,0#177776 ;SETUP PSW
5366 017736 000241 CLC ;TEST INSTRUCTION
5367 017740 022737 030016 177776 CMP #30016,0#177776 ;DID IT CLEAR CARRY BIT
5368 017746 001403 BEQ 1# ;YES GO ON
5369 ;C BIT NOT CLEAR GO TO ERROR
5370 017750 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
5371 017752 000471 .WORD 471 ;UNIQUE ERROR NUMBER
5372 017754 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
5373 017756 1#
5374
5375
5376 017756
5377
5378
5379
5380 017756 TE102:
5381 017756 005267 161022 ;*****
5382 017762 012737 030017 177776 ;*TEST 157 TEST CLN (CLEAR N BIT) INST
5383 017770 000250 ;*****
5384 017772 022737 030007 177776 TST157:
5385 020000 001403 INC #TESTN ;INCREMENT TEST NUMBER
5386 MOV #30017,0#177776 ;SETUP PSW
5387 020002 104000 CLN ;TEST INSTRUCTION
5388 020004 000472 CMP #30007,0#177776 ;DID IT CLEAR NEGATIVE BIT
5389 020006 001127 BEQ 1# ;YES GO ON
5390 020010 ;NO GO TO ERROR
5391 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
5392 .WORD 472 ;UNIQUE ERROR NUMBER
5393 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
5394 1#
5395
5396
5397 020010
5398 020010 005267 160770 TE103:
;*****
;*TEST 160 TEST CLV (CLEAR V BIT) INST
;*****
TST160:
INC #TESTN ;INCREMENT TEST NUMBER

```

```

5399 020014 012737 030017 177776      MOV      #30017,0#177776      ;SETUP PSW
5400 020022 000242                      CLV                          ; TEST INSTRUCTION
5401 020024 022737 030015 177776      CMP      #30015,0#177776     ;DID IT CLEAR OVERFLOW BIT
5402 020032 001403                      BEQ      1#                   ;YES GO ON
5403                                     ;NO GO TO ERROR
5404 020034 104000                      ERROR                       ;ALL ERRORS TO TRAP TO EMT VECTOR
5405 020036 000473                      .WORD   473                  ;UNIQUE ERROR NUMBER
5406 020040 001127                      .WORD   CPUERR              ;ADDRESS OF ERROR MESSAGE
5407 020042

```

1#:

```

5408
5409
5410 020042
5411
5412
5413
5414 020042
5415 020042 005267 160736
5416 020046 012737 030017 177776
5417 020054 000244
5418 020056 022737 030013 177776
5419 020064 001403
5420
5421 020066 104000
5422 020070 000474
5423 020072 001127
5424 020074
5425
5426
5427 020074
5428
5429
5430
5431 020074
5432 020074 005267 160704
5433 020100 012737 030000 177776
5434 020106 000277
5435 020110 022737 030017 177776
5436 020116 001403
5437
5438 020120 104000
5439 020122 000475
5440 020124 001127
5441 020126
5442
5443
5444 020126
5445
5446
5447
5448 020126
5449 020126 005267 160652
5450 020132 012737 030000 177776
5451 020140 000261
5452 020142 022737 030001 177776
5453 020150 001403
5454

```

```

;
;TE104:
;*****
;*TEST 161      TEST CLZ (CLEAR Z BIT) INST
;*****
TST161:

```

```

INC      #TESTN      ;INCREMENT TEST NUMBER
MOV      #30017,0#177776 ;SETUP PSW
CLZ                          ; TEST INSTRUCTION
CMP      #30013,0#177776 ;DID IT CLEAR ZERO BIT
BEQ      1#                   ;YES GO ON
;NO GO TO ERROR
ERROR                       ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD   474                  ;UNIQUE ERROR NUMBER
.WORD   CPUERR              ;ADDRESS OF ERROR MESSAGE

```

1#:

```

;
;TE105:
;*****
;*TEST 162      TEST SCC (SET CONDITION CODES) INST
;*****
TST162:

```

```

INC      #TESTN      ;INCREMENT TEST NUMBER
MOV      #30000,0#177776 ;SETUP PSW
SCC                          ; TEST INSTRUCTION
CMP      #30017,0#177776 ;DID IT SET ALL CONDITION CODE BITS
BEQ      1#                   ;YES GO ON
;NO GO TO ERROR
ERROR                       ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD   475                  ;UNIQUE ERROR NUMBER
.WORD   CPUERR              ;ADDRESS OF ERROR MESSAGE

```

1#:

```

;
;TE106:
;*****
;*TEST 163      TEST SEC (SET C BIT) INST
;*****
TST163:

```

```

INC      #TESTN      ;INCREMENT TEST NUMBER
MOV      #30000,0#177776 ;SETUP PSW
SEC                          ; TEST INSTRUCTION
CMP      #30001,0#177776 ;DID IT SET THE CARRY BIT
BEQ      1#                   ;YES GO ON
;NO GO TO ERROR

```



```

5455 020152 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5456 020154 000476          .WORD      476          ;UNIQUE ERROR NUMBER
5457 020156 001127          .WORD      CPUERR       ;ADDRESS OF ERROR MESSAGE
5458 020160
5459
5460
5461 020160
5462
5463
5464
5465 020160
5466 020160 005267 160620          INC          $TESTN          ;INCREMENT TEST NUMBER
5467 020164 012737 030000 177776      MOV          #30000,0#177776 ;SETUP PSW
5468 020172 000270          SEN          ; TEST INSTRUCTION
5469 020174 022737 030010 177776      CMP          #30010,0#177776 ;DID IT SET THE NEGATIVE BIT
5470 020202 001403          BEQ          1#          ;YES GO ON
5471
5472 020204 104000          ERROR          ;NO GO TO ERROR
5473 020206 000477          .WORD      477          ;ALL ERRORS TO TRAP TO EMT VECTOR
5474 020210 001127          .WORD      CPUERR       ;UNIQUE ERROR NUMBER
5475 020212
5476
5477
5478 020212
5479
5480
5481
5482 020212
5483 020212 005267 160566          INC          $TESTN          ;INCREMENT TEST NUMBER
5484 020216 012737 030000 177776      MOV          #30000,0#177776 ;SETUP PSW
5485 020224 000262          SEV          ; TEST INSTRUCTION
5486 020226 022737 030002 177776      CMP          #30002,0#177776 ;DID IT SET THE OVERFLOW BIT
5487 020234 001403          BEQ          1#          ;YES GO ON
5488
5489 020236 104000          ERROR          ;NO GO TO ERROR
5490 020240 000500          .WORD      500          ;ALL ERRORS TO TRAP TO EMT VECTOR
5491 020242 001127          .WORD      CPUERR       ;UNIQUE ERROR NUMBER
5492 020244
5493
5494
5495 020244
5496
5497
5498
5499 020244
5500 020244 005267 160534          INC          $TESTN          ;INCREMENT TEST NUMBER
5501 020250 012737 030000 177776      MOV          #30000,0#177776 ;SETUP PSW
5502 020256 000264          SEZ          ; TEST INSTRUCTION
5503 020260 022737 030004 177776      CMP          #30004,0#177776 ;DID IT SET THE ZERO BIT
5504 020266 001403          BEQ          1#          ;YES GO ON
5505
5506 020270 104000          ERROR          ;NO GO TO ERROR
5507 020272 000501          .WORD      501          ;ALL ERRORS TO TRAP TO EMT VECTOR
5508 020274 001127          .WORD      CPUERR       ;UNIQUE ERROR NUMBER
5509 020276
5510

```

1#:

TE107:

; *TEST 164 TEST SEN (SET N BIT) INST

TST164:

1#:

TE110:

; *TEST 165 TEST SEV (SET V BIT) INST

TST165:

1#:

TE111:

; *TEST 166 TEST SEZ (SET Z BIT) INST

TST166:

1#:


```

5567
5568 020456 104000          ERROR          ;NO GO TO ERROR
5569 020460 000507          .WORD          ;ALL ERRORS TO TRAP TO EMT VECTOR
5570 020462 001127          .WORD          ;UNIQUE ERROR NUMBER
5571                                     CPUERR        ;ADDRESS OF ERROR MESSAGE
5572 020464 000277          68:  SCC          ;SETUP PSW
5573 020466 000253          .WORD          ; TEST CLN CLC CLV
5574 020470 022737 030004 177776  CMP          #30004,0#177776 ;PSW CORRECT?
5575 020476 001403          BEQ          78          ;YES GO ON
5576                                     ;NO GO TO ERROR
5577 020500 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5578 020502 000510          .WORD          ;UNIQUE ERROR NUMBER
5579 020504 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
5580                                     CPUERR
5581 020506 000277          78:  SCC          ;SETUP PSW
5582 020510 000254          .WORD          ; TEST CLN CLZ
5583 020512 022737 030003 177776  CMP          #30003,0#177776 ;PSW CORRECT?
5584 020520 001403          BEQ          88          ;YES GO ON
5585                                     ;NO GO TO ERROR
5586 020522 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5587 020524 000511          .WORD          ;UNIQUE ERROR NUMBER
5588 020526 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
5589                                     CPUERR
5590 020530 000277          88:  SCC          ;SETUP PSW
5591 020532 000255          .WORD          ; TEST CLN CLC CLZ
5592 020534 022737 030002 177776  CMP          #30002,0#177776 ;PSW CORRECT?
5593 020542 001403          BEQ          98          ;YES GO ON
5594                                     ;NO GO TO ERROR
5595 020544 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5596 020546 000512          .WORD          ;UNIQUE ERROR NUMBER
5597 020550 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
5598                                     CPUERR
5599 020552 000277          98:  SCC          ;SETUP PSW
5600 020554 000256          .WORD          ; TEST CLN CLV CLZ
5601 020556 022737 030001 177776  CMP          #30001,0#177776 ;SETUP PSW
5602 020564 001403          BEQ          108         ;YES GO ON
5603                                     ;NO GO TO ERROR
5604 020566 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR
5605 020570 000513          .WORD          ;UNIQUE ERROR NUMBER
5606 020572 001127          .WORD          ;ADDRESS OF ERROR MESSAGE
5607                                     CPUERR
5608 020574          108:
5609
5610
5611 020574          ;
5612          ;*****
5613          ;*TEST 170      TEST MULTIPLE SETS OF CC BITS
5614          ;*****
5615          TST170:
5616 020574 005267 160204          INC          #TESTN          ;INCREMENT TEST NUMBER
5617 020600 012737 030000 177776  MOV          #30000,0#177776 ;INIT PSW
5618 020606 000263          .WORD          263          ; TEST SEC SEV
5619 020610 022737 030003 177776  CMP          #30003,0#177776 ;PSW CORRECT?
5620 020616 001403          BEQ          18          ;YES GO ON
5621                                     ;NO GO TO ERROR
5622 020620 104000          ERROR          ;ALL ERRORS TO TRAP TO EMT VECTOR

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5679
5680 021002 000257          7#: CCC          ; SETUP PSW
5681 021004 000274          .WORD 274      ; TEST SEN SEZ
5682 021006 022737 030014 177776  CMP #30014,8#177776 ; PSW CORRECT?
5683 021014 001403          BEQ 8#         ; YES GO ON
5684                                     ; NO GO TO ERROR
5685 021016 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5686 021020 000523          .WORD 523      ; UNIQUE ERROR NUMBER
5687 021022 001127          .WORD CPUERR   ; ADDRESS OF ERROR MESSAGE
5688
5689 021024 000257          8#: CCC          ; SETUP PSW
5690 021026 000275          .WORD 275      ; TEST SEN SEC SEZ
5691 021030 022737 030015 177776  CMP #30015,8#177776 ; PSW CORRECT?
5692 021036 001403          BEQ 9#         ; YES GO ON
5693                                     ; NO GO TO ERROR
5694 021040 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5695 021042 000524          .WORD 524      ; UNIQUE ERROR NUMBER
5696 021044 001127          .WORD CPUERR   ; ADDRESS OF ERROR MESSAGE
5697
5698 021046 000257          9#: CCC          ; SETUP PSW
5699 021050 000276          .WORD 276      ; TEST SEN SEV SEZ
5700 021052 022737 030016 177776  CMP #30016,8#177776 ; PSW CORRECT?
5701 021060 001403          BEQ 10#        ; YES GO ON
5702                                     ; NO GO TO ERROR
5703 021062 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5704 021064 000525          .WORD 525      ; UNIQUE ERROR NUMBER
5705 021066 001127          .WORD CPUERR   ; ADDRESS OF ERROR MESSAGE
5706
5707 021070          10#:
5708
5709
5710 021070          ;
5711          ;TE113A:
5712          ;*****
5713          ;*TEST 171      TEST SIGNED AND CONDITIONAL BRANCHES
5714          ;*****
5715          ;TST171:
5716 021070 005267 157710      INC #TESTN      ; INCREMENT TEST NUMBER
5717 021074 000257          CCC            ; CLEAR ALL CC BITS IN PSW
5718 021076 002003          BGE 1#         ; BGE SHOULD BRANCH
5719                                     ; ERROR! DIDN'T BRANCH
5720 021100 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5721 021102 000526          .WORD 526      ; UNIQUE ERROR NUMBER
5722 021104 001127          .WORD CPUERR   ; ADDRESS OF ERROR MESSAGE
5723
5724 021106 003003          1#: BGT 2#       ; BGT SHOULD BRANCH
5725                                     ; ERROR! DIDN'T BRANCH
5726 021110 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5727 021112 000527          .WORD 527      ; UNIQUE ERROR NUMBER
5728 021114 001127          .WORD CPUERR   ; ADDRESS OF ERROR MESSAGE
5729
5729 021116 003401          2#: BLE 3#     ; BLE SHOULDN'T BRANCH
5730 021120 000403          BR 4#         ; BRANCH TO NEXT TEST
5731                                     ; ERROR! BLE SHOULD NOT HAVE BRANCHED
5732
5732 021122          3#:
5733 021122 104000          ERROR          ; ALL ERRORS TO TRAP TO EMT VECTOR
5734 021124 000530          .WORD 530      ; UNIQUE ERROR NUMBER

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5735	021126	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5736							
5737	021130	002401	4:	BLT	5:		;BLT SHOULD NOT BRANCH
5738	021132	000403		BR	6:		;BRANCH TO NEXT TEST
5739							;ERROR; BLT SHOULD NOT HAVE BRANCHED
5740	021134		5:				
5741	021134	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5742	021136	000531		.WORD	531		;UNIQUE ERROR NUMBER
5743	021140	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5744							
5745	021142	000264	6:	SEZ			;SET THE Z BIT IN PSW
5746	021144	003403		BLE	7:		;BLE SHOULD BRANCH
5747							;ERROR; BLE DIDN'T BRANCH
5748	021146	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5749	021150	000532		.WORD	532		;UNIQUE ERROR NUMBER
5750	021152	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5751							
5752	021154	003001	7:	BGT	8:		;BGT SHOULD NOT BRANCH
5753	021156	000403		BR	9:		;BRANCH TO NEXT TEST
5754							;ERROR; BGT SHOULD NOT HAVE BRANCHED
5755	021160		8:				
5756	021160	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5757	021162	000533		.WORD	533		;UNIQUE ERROR NUMBER
5758	021164	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5759							
5760	021166	000257	9:	CCC			;CLEAR ALL CC BITS IN PSW
5761	021170	000270		SEN			;SET N BIT IN PSW
5762	021172	002403		BLT	10:		;SHOULD BRANCH TO NEXT TEST
5763							;ERROR; BLT SHOULD HAVE BRANCHED
5764	021174	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5765	021176	000534		.WORD	534		;UNIQUE ERROR NUMBER
5766	021200	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5767							
5768	021202	003403	10:	BLE	11:		;SHOULD BRANCH TO NEXT TEST
5769							;ERROR; BLE SHOULD HAVE BRANCHED
5770	021204	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5771	021206	000535		.WORD	535		;UNIQUE ERROR NUMBER
5772	021210	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5773							
5774	021212	002001	11:	BGE	12:		;BGE SHOULD NOT BRANCH
5775	021214	000403		BR	13:		;BRANCH TO NEXT TEST
5776							;ERROR; BGE SHOULD NOT HAVE BRANCHED
5777	021216		12:				
5778	021216	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5779	021220	000536		.WORD	536		;UNIQUE ERROR NUMBER
5780	021222	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5781							
5782	021224	003001	13:	BGT	14:		;BGT SHOULD NOT BRANCH
5783	021226	000403		BR	15:		;BRANCH TO NEXT TEST
5784							;ERROR; BGT SHOULD NOT HAVE BRANCHED
5785	021230		14:				
5786	021230	104000		ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
5787	021232	000537		.WORD	537		;UNIQUE ERROR NUMBER
5788	021234	001127		.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
5789							
5790	021236	000257	15:	CCC			;CLEAR ALL CC BITS


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5903
5904 021546 016700 156626
5905 021552 022700 000001
5906 021556 001403
5907
5908 021560 104000
5909 021562 000553
5910 021564 001127
5911
5912 021566 022701 000002
5913 021572 001403
5914
5915 021574 104000
5916 021576 000554
5917 021600 001127
5918
5919 021602 022702 000003
5920 021606 001403
5921
5922 021610 104000
5923 021612 000555
5924 021614 001127
5925
5926 021616 022703 000004
5927 021622 001403
5928
5929 021624 104000
5930 021626 000556
5931 021630 001127
5932
5933 021632 022704 000005
5934 021636 001403
5935
5936 021640 104000
5937 021642 000557
5938 021644 001127
5939
5940 021646 022705 000006
5941 021652 001403
5942
5943 021654 104000
5944 021656 000560
5945 021660 001127
5946
5947 021662 000207
5948
5949 021664
5950
5951
5952
5953 021664
5954 021664 005267 157114
5955 021670 005000
5956 021672 005001
5957 021674 005002
5958 021676 005003

      MOV      400,R0
      TA114:  CMP      #1,R0
      BEQ      TB114
      ;RESTORE R0
      ;CHECK R0
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      ERROR   .WORD   553
      .WORD   CPUERR

      TB114:  CMP      #2,R1
      BEQ      TC114
      ;CHECK R1
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      ERROR   .WORD   554
      .WORD   CPUERR

      TC114:  CMP      #3,R2
      BEQ      TD114
      ;CHECK R2
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      ERROR   .WORD   555
      .WORD   CPUERR

      TD114:  CMP      #4,R3
      BEQ      TF114
      ;CHECK R3
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      ERROR   .WORD   556
      .WORD   CPUERR

      TF114:  CMP      #5,R4
      BEQ      TG114
      ;CHECK R4
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      ERROR   .WORD   557
      .WORD   CPUERR

      TG114:  CMP      #6,R5
      BEQ      TH114
      ;CHECK R5
      ;OK GO ON
;ERROR; BLT SHOULD NOT HAVE BRANCHED
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

      TH114:  RTS      PC
      ;RETURN

;FINNOP:
;*****
;*TEST 173      TEST ATERNATE REGISTER SET
;*****
TST173:
      INC      #TESTN
      CLR      R0
      CLR      R1
      CLR      R2
      CLR      R3
      ;INCREMENT TEST NUMBER
      ;-----CLEAR-----
      ;-----PRIMARY-----
      ;-----GENERAL-----
      ;-----PURPOSE-----
    
```



```

6071 022236
6072
6073
6074
6075 022236
6076 022236 005267 156542
6077 022242 012700 177777
6078 022246 020027 177777
6079 022252 001403
6080
6081 022254 104000
6082 022256 000577
6083 022260 001127
6084 022262 005000
6085 022264 020027 000000
6086 022270 001403
6087
6088 022272 104000
6089 022274 000600
6090 022276 001127
6091 022300 012700 125252
6092 022304 020027 125252
6093 022310 001403
6094
6095 022312 104000
6096 022314 000601
6097 022316 001127
6098 022320 012700 052525
6099 022324 020027 052525
6100 022330 001403
6101
6102 022332 104000
6103 022334 000602
6104 022336 001127
6105 022340
6106
6107
6108 022340
6109
6110
6111
6112 022340
6113 022340 005267 156440
6114 022344 012701 177777
6115 022350 020127 177777
6116 022354 001403
6117
6118 022356 104000
6119 022360 000603
6120 022362 001127
6121 022364 005001
6122 022366 020127 000000
6123 022372 001403
6124
6125 022374 104000
6126 022376 000604

```

```

ALROTS:
;*****
;*TEST 174 ALTERNATE REGISTER SET R0 BIT TESTS
;*****
TST174:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      MOV      $177777,R0     ;R0=177777
      CMP      R0,$177777     ;DOES R0=177777
      BEQ      1$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   577            ;UNIQUE ERROR NUMBER
      .WORD   CPUERR        ;ADDRESS OF ERROR MESSAGE
1$:   CLR      R0              ;R0=0
      CMP      R0,#0         ;DOES R0=0
      BEQ      2$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   600            ;UNIQUE ERROR NUMBER
      .WORD   CPUERR        ;ADDRESS OF ERROR MESSAGE
2$:   MOV      $125252,R0     ;R0=125252
      CMP      R0,$125252    ;DOES R0=125252
      BEQ      3$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   601            ;UNIQUE ERROR NUMBER
      .WORD   CPUERR        ;ADDRESS OF ERROR MESSAGE
3$:   MOV      $52525,R0     ;R0=52525
      CMP      R0,$52525    ;DOES R0=52525
      BEQ      4$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   602            ;UNIQUE ERROR NUMBER
      .WORD   CPUERR        ;ADDRESS OF ERROR MESSAGE
4$:
;
;ALR1TS:
;*****
;*TEST 175 ALTERNATE REGISTER SET R1 BIT TESTS
;*****
TST175:
      INC      $TESTN          ;INCREMENT TEST NUMBER
      MOV      $177777,R1     ;R1=177777
      CMP      R1,$177777    ;DOES R1=177777
      BEQ      1$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   603            ;UNIQUE ERROR NUMBER
      .WORD   CPUERR        ;ADDRESS OF ERROR MESSAGE
1$:   CLR      R1              ;R1=0
      CMP      R1,#0         ;DOES R1=0
      BEQ      2$            ;YES GO ON
                               ;NO GO TO ERROR
      ERROR    ;ALL ERRORS TO TRAP TO EMT VECTOR
      .WORD   604            ;UNIQUE ERROR NUMBER

```


ALTERNATE REGISTER SET R1 BIT TESTS

```

6127 022400 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6128 022402 012701 125252 2#:  MOV    #125252,R1      ;R1=125252
6129 022406 020127 125252   CMP    R1,#125252      ;DOES R1=125252
6130 022412 001403          BEQ    3#              ;YES GO ON
6131                                     ;NO GO TO ERROR
6132 022414 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6133 022416 000605          .WORD  605             ;UNIQUE ERROR NUMBER
6134 022420 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6135 022422 012701 052525 3#:  MOV    #52525,R1      ;R1=52525
6136 022426 020127 052525   CMP    R1,#52525      ;DOES R1=52525
6137 022432 001403          BEQ    4#              ;YES GO ON
6138                                     ;NO GO TO ERROR
6139 022434 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6140 022436 000606          .WORD  606             ;UNIQUE ERROR NUMBER
6141 022440 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6142 022442          4#:
6143
6144
6145 022442          ;
6146          ;ALR2TS:
6147          ;*****
6148          ;*TEST 176      ALTERNATE REGISTER SET R2 BIT TESTS
6149          ;*****
6150 022442 005267 156336  TST176:
6151 022446 012702 177777   INC    #TESTN          ;INCREMENT TEST NUMBER
6152 022452 020227 177777   MOV    #177777,R2     ;R2=177777
6153 022456 001403          CMP    R2,#177777     ;DOES R2=177777
6154                                     BEQ    1#              ;YES GO ON
6155                                     ;NO GO TO ERROR
6156 022460 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6157 022462 000607          .WORD  607             ;UNIQUE ERROR NUMBER
6158 022464 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6159 022470 020227 000000 1#:  CLR    R2              ;R2=0
6160 022474 001403          CMP    R2,#0          ;DOES R2=0
6161                                     BEQ    2#              ;YES GO ON
6162                                     ;NO GO TO ERROR
6163 022476 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6164 022500 000610          .WORD  610             ;UNIQUE ERROR NUMBER
6165 022502 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6166 022504 012702 125252 2#:  MOV    #125252,R2     ;R2=125252
6167 022510 020227 125252   CMP    R2,#125252    ;DOES R2=125252
6168                                     BEQ    3#              ;YES GO ON
6169                                     ;NO GO TO ERROR
6170 022516 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6171 022520 000611          .WORD  611             ;UNIQUE ERROR NUMBER
6172 022522 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6173 022524 012702 052525 3#:  MOV    #52525,R2     ;R2=52525
6174 022530 020227 052525   CMP    R2,#52525     ;DOES R2=52525
6175                                     BEQ    4#              ;YES GO ON
6176                                     ;NO GO TO ERROR
6177 022536 104000          ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
6178 022540 000612          .WORD  612             ;UNIQUE ERROR NUMBER
6179 022542 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6180                                     4#:
6181
6182 022544          ;ALR3TS:

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6183
6184
6185
6186 022544
6187 022544 005267 156234
6188 022550 012703 177777
6189 022554 020327 177777
6190 022560 001403
6191
6192 022562 104000
6193 022564 000613
6194 022566 001127
6195 022570 005003
6196 022572 020327 000000
6197 022576 001403
6198
6199 022600 104000
6200 022602 000614
6201 022604 001127
6202 022606 012703 125252
6203 022612 020327 125252
6204 022616 001403
6205
6206 022620 104000
6207 022622 000615
6208 022624 001127
6209 022626 012703 052525
6210 022632 020327 052525
6211 022636 001403
6212
6213 022640 104000
6214 022642 000616
6215 022644 001127
6216 022646
6217
6218
6219 022646
6220
6221
6222
6223 022646
6224 022646 005267 156132
6225 022652 012704 177777
6226 022656 020427 177777
6227 022662 001403
6228
6229 022664 104000
6230 022666 000617
6231 022670 001127
6232 022672 005004
6233 022674 020427 000000
6234 022700 001403
6235
6236 022702 104000
6237 022704 000620
6238 022706 001127

```

```

*****
; *TEST 177 ALTERNATE REGISTER SET R3 BIT TESTS
*****
TST177:
      INC      $TESTN          ; INCREMENT TEST NUMBER
      MOV      #177777,R3     ; R3=177777
      CMP      R3,#177777     ; DOES R3=177777
      BEQ      1$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   613             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE
1$:   CLR      R3              ; R3=0
      CMP      R3,#0         ; DOES R3=0
      BEQ      2$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   614             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE
2$:   MOV      #125252,R3    ; R3=125252
      CMP      R3,#125252   ; DOES R3=125252
      BEQ      3$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   615             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE
3$:   MOV      #52525,R3     ; R3=52525
      CMP      R3,#52525   ; DOES R3=52525
      BEQ      4$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   616             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE
4$:
;
; ALR4TS:
*****
; *TEST 200 ALTERNATE REGISTER SET R4 BIT TESTS
*****
TST200:
      INC      $TESTN          ; INCREMENT TEST NUMBER
      MOV      #177777,R4     ; R4=177777
      CMP      R4,#177777   ; DOES R4=177777
      BEQ      1$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   617             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE
1$:   CLR      R4              ; R4=0
      CMP      R4,#0         ; DOES R4=0
      BEQ      2$            ; YES GO ON
                               ; NO GO TO ERROR
                               ; ALL ERRORS TO TRAP TO EMT VECTOR
      ERROR   620             ; UNIQUE ERROR NUMBER
      .WORD   CPUERR         ; ADDRESS OF ERROR MESSAGE

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6239 022710 012704 125252      20:  MOV    #125252,R4      ;R4=125252
6240 022714 020427 125252      CMP    R4,#125252     ;DOES R4=125252
6241 022720 001403                BEQ    30             ;YES GO ON
6242                                ;NO GO TO ERROR
6243 022722 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6244 022724 000621                .WORD ;UNIQUE ERROR NUMBER
6245 022726 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6246 022730 012704 052525      30:  MOV    #52525,R4      ;R4=52525
6247 022734 020427 052525      CMP    R4,#52525     ;DOES R4=52525
6248 022740 001403                BEQ    40             ;YES GO ON
6249                                ;NO GO TO ERROR
6250 022742 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6251 022744 000622                .WORD ;UNIQUE ERROR NUMBER
6252 022746 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6253 022750
6254
6255
6256 022750
6257
6258
6259
6260 022750
6261 022750 005267 156030      TST201: INC    #TESTN          ;INCREMENT TEST NUMBER
6262 022754 012705 177777      MOV    #177777,R5    ;R5=177777
6263 022760 020527 177777      CMP    R5,#177777    ;DOES R5=177777
6264 022764 001403                BEQ    10             ;YES GO ON
6265                                ;NO GO TO ERROR
6266 022766 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6267 022770 000623                .WORD ;UNIQUE ERROR NUMBER
6268 022772 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6269 022774 005005                CLR    R5             ;R5=0
6270 022776 020527 000000      10:  CMP    R5,#0         ;DOES R5=0
6271 023002 001403                BEQ    20             ;YES GO ON
6272                                ;NO GO TO ERROR
6273 023004 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6274 023006 000624                .WORD ;UNIQUE ERROR NUMBER
6275 023010 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6276 023012 012705 125252      20:  MOV    #125252,R5    ;R5=125252
6277 023016 020527 125252      CMP    R5,#125252    ;DOES R5=125252
6278 023022 001403                BEQ    30             ;YES GO ON
6279                                ;NO GO TO ERROR
6280 023024 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6281 023026 000625                .WORD ;UNIQUE ERROR NUMBER
6282 023030 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6283 023032 012705 052525      30:  MOV    #52525,R5    ;R5=52525
6284 023036 020527 052525      CMP    R5,#52525     ;DOES R5=52525
6285 023042 001403                BEQ    40             ;YES GO ON
6286                                ;NO GO TO ERROR
6287 023044 104000                ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6288 023046 000626                .WORD ;UNIQUE ERROR NUMBER
6289 023050 001127                .WORD ;ADDRESS OF ERROR MESSAGE
6290 023052 042767 004000 154716 40:  BIC    #BIT11,PS     ;RETURN TO PRIMARY GEN PURPOSE REGS
6291
6292
6293 023060
6294

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```

6295 ;*TEST 202 TEST MPFS (MOVE FROM PROCESSOR STATUS) INST
6296 ;*****
6297 023060 005267 155720 TST202: INC #TESTN ;INCREMENT TEST NUMBER
6298 023060 005004 CLR R4 ;SETUP DESTINATION R4
6299 023064 005004
6300
6301 023066 012701 023330 MOV #TE115A,R1 ;SETUP POINTERS TO TABLES
6302 023072 012702 023340 MOV #TE115B,R2 ;
6303 023076 012703 023346 MOV #TE115C,R3 ;
6304 023102 012137 177776 18: MOV (R1),#0177776 ;SETUP PSW
6305 023106 106704 HFPS R4 ; TEST INSTRUCTION
6306 023110 023722 177776 CMP #0177776,(R2) ;CHECK PSW
6307 023114 001403 BEQ 28 ;OK GO ON
6308 ;NO GO TO ERROR
6309 023116 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6310 023120 000627 .WORD 627 ;UNIQUE ERROR NUMBER
6311 023122 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6312
6313 023124 020423 28: CMP R4,(R3) ;CHECK R4
6314 023126 001403 BEQ 38 ;OK GO ON
6315 ;NO GO TO ERROR
6316 023130 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6317 023132 000630 .WORD 630 ;UNIQUE ERROR NUMBER
6318 023134 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6319
6320 023136 021127 177777 38: CMP (R1),#177777 ;ARE WE DONE
6321 023142 001357 BNE 18 ;NO GO TO 18
6322
6323
6324 023144 012701 023330 MOV #TE115A,R1 ;SETUP POINTERS TO TABLES
6325 023150 012702 023340 MOV #TE115B,R2 ;
6326 023154 012703 023346 MOV #TE115C,R3 ;
6327 023160 010605 MOV R6,R5 ;SAVE STACK IN R5
6328 023162 011137 177776 1018: MOV (R1),#0177776 ;SETUP PSW
6329 023166 106706 HFPS R6 ; TEST INSTRUCTION
6330 023170 023712 177776 CMP #0177776,(R2) ;CHECK PSW
6331 023174 001403 BEQ 1028 ;OK GO ON
6332 ;NO GO TO ERROR
6333 023176 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6334 023200 000631 .WORD 631 ;UNIQUE ERROR NUMBER
6335 023202 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6336
6337 023204 020613 1028: CMP R6,(R3) ;CHECK R6
6338 023206 001403 BEQ 1038 ;OK GO ON
6339 ;NO GO TO ERROR
6340 023210 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6341 023212 000632 .WORD 632 ;UNIQUE ERROR NUMBER
6342 023214 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6343
6344 023216 010506 1038: MOV R5,R6 ;RESTORE STACK
6345
6346
6347 023220 012701 023330 MOV #TE115A,R1 ;SETUP POINTERS TO TABLES
6348 023224 012702 023340 MOV #TE115B,R2 ;
6349 023230 012703 023354 MOV #TE115D,R3 ;
6350 023234 005037 001034 CLR #EXPDAT ;INIT EXPECTED DATA HOLDER.

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6351 023240 012704 001034      4:  MOV    #EXPDAT,R4      ;SETUP POINTER TO TEST LOCATION
6352 023244 012137 177776      MOV    (R1),#0177776    ;SETUP PSW
6353 023250 106724              MFPS   (R4)             ; TEST INSTRUCTION
6354 023252 023722 177776      CMP    #0177776,(R2)    ;CHECK PSW
6355 023256 001403              BEQ    5#               ;OK GO ON
6356                                ;NO GO TO ERROR
6357 023260 104000              ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6358 023262 000633              .WORD 633              ;UNIQUE ERROR NUMBER
6359 023264 001127              .WORD CPUERR           ;ADDRESS OF ERROR MESSAGE
6360
6361 023266 020427 001035      5:  CMP    R4,#EXPDAT+1    ;CHECK R4
6362 023272 001403              BEQ    6#               ;OK GO ON
6363                                ;NO GO TO ERROR
6364 023274 104000              ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6365 023276 000634              .WORD 634              ;UNIQUE ERROR NUMBER
6366 023300 001127              .WORD CPUERR           ;ADDRESS OF ERROR MESSAGE
6367
6368 023302 023723 001034      6:  CMP    #EXPDAT,(R3)    ;CHECK TEST LOCATION
6369 023306 001403              BEQ    7#               ;OK GO ON
6370                                ;NO GO TO ERROR
6371 023310 104000              ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6372 023312 000635              .WORD 635              ;UNIQUE ERROR NUMBER
6373 023314 001127              .WORD CPUERR           ;ADDRESS OF ERROR MESSAGE
6374 023316 021127 177777      7:  CMP    (R1),#177777    ;ARE WE DONE
6375 023322 001346              BNE    4#               ;NO GO TO 4#
6376
6377 023324 000167 000032      JMP    TE115F
6378
6379
6380
6381 023330 030207      ;
6382 023332 030000      ;
6383 023334 030057      ;
6384 023336 177777      ;
6385 023340 030211      TE115A: .WORD 30207
6386 023342 030004      .WORD 30000
6387 023344 030041      .WORD 30057
6388 023346 177607      .WORD 177777
6389 023350 000000      TE115B: .WORD 30211
6390 023352 000057      .WORD 30004
6391 023354 000207      .WORD 30041
6392 023356 000000      TE115C: .WORD 177607
6393 023360 000057      .WORD 0
6394 023362 000240      .WORD 57
6395                                TE115D: .WORD 207
6396                                .WORD 0
6397                                .WORD 57
6398                                TE115F: NOP
6399                                ;
6400                                ;
6401 023364 005267 155414      ;*****
6402                                ;*TEST 203 TEST MTPS (MOVE TO PROCESSOR STATUS) INST
6403                                ;*****
6404                                TST203:
6405                                INC    #TESTN          ;INCREMENT TEST NUMBER
6406 023370 012737 030000 177776      MOV    #30000,#177776  ;SET PSW TO KERNEL MODE
6407 023376 012701 023722      MOV    #TE116D,R1      ;SETUP POINTERS TO TABLES
6408 023402 012702 023700      MOV    #TE116B,R2
6409 023406 010103      MOV    R1,R3

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6407	023410	004767	000142		JSR	PC.T116		; TEST INSTRUCTION AND CHECK PSW ; AND SOURCE OPERAND
6408								
6409								
6410								
6411	023414	012737	140000	177776	MOV	#140000,#177776		; SET PSW TO USER MODE
6412	023422	012706	000600		MOV	#600,R6		; SETUP USER STACK
6413	023426	012701	023722		MOV	#TE116D,R1		; SETUP POINTERS TO TABLES
6414	023432	012702	023712		MOV	#TE116C,R2		
6415	023436	010103			MOV	R1,R3		
6416	023440	004767	000112		JSR	PC.T116		; TEST INSTRUCTION AND CHECK PSW ; AND SOURCE OPERAND
6417								
6418								
6419								
6420	023444	012737	140000	177776	MOV	#140000,#177776		; SET PSW TO USER MODE AND CLEAR CC BITS
6421	023452	012701	023674		MOV	#TE116A,R1		; SETUP POINTERS TO TABLES
6422	023456	012702	023712		MOV	#TE116C,R2		
6423	023462	012703	023722		MOV	#TE116D,R3		
6424	023466	010104			MOV	R1,R4		; SAVE A COPY OF R1 INTO R4
6425	023470	004767	000124		JSR	PC.TA116		; TEST INSTRUCTION AND CHECK PSW ; AND SOURCE OPERAND
6426								
6427								
6428								
6429	023474	012737	030000	177776	MOV	#30000,#177776		; SET PSW TO KERNEL MODE
6430	023502	012701	023674		MOV	#TE116A,R1		; SETUP POINTERS TO TABLES
6431	023506	012702	023700		MOV	#TE116B,R2		
6432	023512	012703	023722		MOV	#TE116D,R3		
6433	023516	010104			MOV	R1,R4		; SAVE A COPY OF R1 INTO R4
6434	023520	004767	000074		JSR	PC.TA116		; TEST INSTRUCTION AND CHECK PSW ; AND SOURCE OPERAND
6435								
6436								
6437	023524	005037	177776		CLR	#177776		; SET PSW TO KERNEL MODE
6438	023530	106427	177412		MTPS	#177412		; TEST INSTRUCTION
6439	023534	022737	000012	177776	CMF	#12,#177776		; IS PSW CORRECT
6440	023542	001403			BEQ	100#		; YES GO ON
6441								; NO GO TO ERROR
6442	023544	104000			ERROR			; ALL ERRORS TO TRAP TO EMT VECTOR
6443	023546	000636			.WORD	636		; UNIQUE ERROR NUMBER
6444	023550	001127			.WORD	CPUERR		; ADDRESS OF ERROR MESSAGE
6445	023552							
6446								
6447	023552	000167	000154		JMP	FIN116		
6448								
6449	023556	012105						
6450	023560	106405			MOV	(R1)+,R5		; MOVE TEST DATA TO R5
6451	023562	023722	177776		MTPS	R5		; TEST INSTRUCTION
6452	023566	001403			CMF	#177776,(R2)+		; IS PSW CORRECT
6453					BEQ	1#		; YES GO ON
6454	023570	104000			ERROR			; NO GO TO ERROR
6455	023572	000637			.WORD	637		; ALL ERRORS TO TRAP TO EMT VECTOR
6456	023574	001127			.WORD	CPUERR		; UNIQUE ERROR NUMBER
6457								; ADDRESS OF ERROR MESSAGE
6458	023576	022305						
6459	023600	001403			CMF	(R3)+,R5		; IS R5 CORRECT
6460					BEQ	2#		; YES GO ON
6461	023602	104000			ERROR			; NO GO TO ERROR
6462	023604	000640			.WORD	640		; ALL ERRORS TO TRAP TO EMT VECTOR
								; UNIQUE ERROR NUMBER


```

6463 023606 001127          .WORD  CPUERR          ;ADDRESS OF ERROR MESSAGE
6464
6465 023610 021227 177777  2#:  CMP      (R2),#177777  ;ARE WE DONE
6466 023614 001360          BNE      T116             ;NO GO TO T116
6467 023616 000207          RTS      PC              ;RETURN
6468
6469 023620 106421          |TA116: MTPS      (R1),    ; TEST INSTRUCTION
6470 023622 023722 177776  CMP      @#177776,(R2),  ;IS PSW CORRECT
6471 023626 001403          BEQ      1#              ;YES GO ON
6472
6473 023630 104000          ERROR   ;NO GO TO ERROR
6474 023632 000641          .WORD   641             ;ALL ERRORS TO TRAP TO EMT VECTOR
6475 023634 001127          .WORD   CPUERR         ;UNIQUE ERROR NUMBER
6476
6477 023636 122423          1#:  CMPB     (R4),.(R3),  ;CHECK TEST LOCATION
6478 023640 001403          BEQ     2#              ;OK GO ON
6479
6480 023642 104000          ERROR   ;NO GO TO ERROR
6481 023644 000642          .WORD   642             ;ALL ERRORS TO TRAP TO EMT VECTOR
6482 023646 001127          .WORD   CPUERR         ;UNIQUE ERROR NUMBER
6483
6484 023650 020104          2#:  CMP      R1,R4      ;IS SOURCE OPERAND CORRECT
6485 023652 001403          BEQ     3#              ;YES GO ON
6486
6487 023654 104000          ERROR   ;NO GO TO ERROR
6488 023656 000643          .WORD   643             ;ALL ERRORS TO TRAP TO EMT VECTOR
6489 023660 001127          .WORD   CPUERR         ;UNIQUE ERROR NUMBER
6490
6491 023662 005203          3#:  INC      R3          ;POINT TO NEXT WORD
6492 023664 021227 177777  CMP      (R2),#177777  ;ARE WE DONE
6493 023670 001353          BNE      TA116         ;NO GO TO TA116
6494 023672 000207          RTS      PC              ;RETURN
6495
6496 023674          377          |TE116A: .BYTE   377
6497 023675          000          .BYTE   0
6498 023676          252          .BYTE   252
6499 023677          125          .BYTE   125
6500 023700 030357          TE116B: .WORD   30357
6501 023702 030000          .WORD   30000
6502 023704 030252          .WORD   30252
6503 023706 030105          .WORD   30105
6504 023710 177777          .WORD   177777
6505 023712 140017          TE116C: .WORD   140017
6506 023714 140000          .WORD   140000
6507 023716 140012          .WORD   140012
6508 023720 140005          .WORD   140005
6509 023722 177777          TE116D: .WORD   177777
6510 023724 177400          .WORD   177400
6511 023726 177652          .WORD   177652
6512 023730 177525          .WORD   177525
6513
6514 023732          |FIN116:
6515
6516 023732          |TE117:
6517
6518          ;*****
          ;*TEST 204          TEST MFPT (MOVE FROM PROCESSOR TYPE)

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6519
6520 023732      ;*****
6521 023732      TST204:
6522 023736 005267 155046      INC      #TESTN      ;INCREMENT TEST NUMBER
6523 023742 013746 000010      MOV      @#10,-(SP)  ;SAVE VECTOR
6524 023750 012737 024070 000010      MOV      @TE117A,@#10 ;SETUP VECTOR TO HANDLE POSSIBLE ILLEGAL INST TR
6525 023754 012737 030000 177776      MOV      @177777,RO  ;INIT RO
6526 023762 000007      MOV      @30000,@#177776 ;SETUP PSW
6527 023764 022737 030000 177776      .WORD   7            ; TEST INSTRUCTION
6528 023772 001403      CMP      @30000,@#177776 ;IS PSW CORRECT
6529      BEQ      1#      ;YES GO ON
6530      ERROR      ;NO GO TO ERROR
6531 023774 104000      .WORD   644          ;ALL ERRORS TO TRAP TO EMT VECTOR
6532 024000 001127      .WORD   CPUERR      ;UNIQUE ERROR NUMBER
6533 024002 020027 000005      1#:  CMP      RO,#5    ;ADDRESS OF ERROR MESSAGE
6534 024006 001403      BEQ      2#      ;IS RO CORRECT
6535      ERROR      ;YES GO ON
6536 024010 104000      .WORD   645          ;NO GO TO ERROR
6537 024012 000645      .WORD   CPUERR      ;ALL ERRORS TO TRAP TO EMT VECTOR
6538 024014 001127      .WORD   CPUERR      ;UNIQUE ERROR NUMBER
6539      ERROR      ;ADDRESS OF ERROR MESSAGE
6540 024016 012700 177777      2#:  MOV      @177777,RO  ;INIT RO
6541 024022 000277      SCC      ;SET ALL CC BITS
6542 024024 000007      .WORD   7            ; TEST INSTRUCTION
6543 024026 022737 030017 177776      CMP      @30017,@#177776 ;IS PSW CORRECT
6544 024034 001403      BEQ      3#      ;YES GO ON
6545      ERROR      ;NO GO TO ERROR
6546 024036 104000      .WORD   646          ;ALL ERRORS TO TRAP TO EMT VECTOR
6547 024040 000646      .WORD   CPUERR      ;UNIQUE ERROR NUMBER
6548 024042 001127      .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
6549      ERROR      ;IS RO CORRECT
6550 024044 020027 000005      3#:  CMP      RO,#5    ;YES GO ON
6551 024050 001403      BEQ      4#      ;NO GO TO ERROR
6552      ERROR      ;ALL ERRORS TO TRAP TO EMT VECTOR
6553 024052 104000      .WORD   647          ;UNIQUE ERROR NUMBER
6554 024054 000647      .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
6555 024056 001127      .WORD   CPUERR
6556      ERROR      ;ADDRESS OF ERROR MESSAGE
6557 024060 012637 000010      4#:  MOV      (SP),@#10 ;RESTORE VECTOR
6558      JMP      FIN117
6559 024064 000167 000006
6560
6561      ;
6562 024070      TE117A:
6563 024070 104000      ERROR
6564 024072 000650      .WORD   650          ;ERROR! GO TO ERROR IF TRAP TAKES PLACE
6565 024074 001127      .WORD   CPUERR      ;ALL ERRORS TO TRAP TO EMT VECTOR
6566      .WORD   CPUERR      ;UNIQUE ERROR NUMBER
6567      .WORD   CPUERR      ;ADDRESS OF ERROR MESSAGE
6568 024076      ;
6569      FIN117:
6570 024076      ;
6571      TE120:
6572      ;*****
6573      ;*TEST 205      TEST MALT (NOT KERNEL MODE)
6574 024076      ;*****
        TST205:
    
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6575 024076 005267 154702          INC      #TESTN          ; INCREMENT TEST NUMBER
6576 024102 005037 177766          CLR      @#177766       ; INIT CPU ERROR REG
6577 024106 005037 177776          CLR      @#177776       ; INIT PSW-SET KERNEL MODE
6578 024112 013746 000004          MOV      @#4,-(SP)      ; SAVE VECTOR
6579 024116 013746 000006          MOV      @#6,-(SP)      ; SAVE VECTOR
6580 024122 012737 024162 000004   MOV      @TE120A,@#4    ; SET UP VECTOR TO HANDLE ILLEGAL HALT
6581 024130 005037 000006          CLR      @#6           ; SET UP VECTOR TO COME BACK IN KERNEL MODE
6582 024134 012767 140000 153634   MOV      @#140000,PS    ; SET IN USER MODE
6583 024142 012706 000600          MOV      @#600,R6      ; INITIALIZE THE USER STACK POINTER
6584 024146 000000          HALT                    ; TEST INSTRUCTION
6585                                     ; ERROR! IF NOTHING HAPPENED GO TO ERROR
6586 024150          PROCNT:
6587 024150 104000          ERROR    ; ALL ERRORS TO TRAP TO EMT VECTOR
6588 024152 000651          .WORD   651           ; UNIQUE ERROR NUMBER
6589 024154 001127          .WORD   CPUERR        ; ADDRESS OF ERROR MESSAGE
6590
6591 024156 000167 000064          JMP      FIN120        ;
6592
6593                                     ;
6594 024162 022737 030000 177776   TE120A: CMP      @#30000,@#177776 ; IS PSW CORRECT/PREVIOUS MODE = USER?
6595 024170 001403          BEQ     1#           ; YES GO ON
6596                                     ; NO, GO TO ERROR
6597 024172 104000          ERROR    ; ALL ERRORS TO TRAP TO EMT VECTOR
6598 024174 000652          .WORD   652           ; UNIQUE ERROR NUMBER
6599 024176 001127          .WORD   CPUERR        ; ADDRESS OF ERROR MESSAGE
6600
6601 024200 022737 000200 177766 1# : CMP      @#200,@#177766 ; TEST CPU ERROR REGISTER
6602 024206 001403          BEQ     2#           ; YES GO ON
6603                                     ; NO, GO TO ERROR
6604 024210 104000          ERROR    ; ALL ERRORS TO TRAP TO EMT VECTOR
6605 024212 000653          .WORD   653           ; UNIQUE ERROR NUMBER
6606 024214 001127          .WORD   CPUERR        ; ADDRESS OF ERROR MESSAGE
6607
6608 024216 022627 024150          2# : CMP      (SP)+,@#PROCNT ; DOES STACK CONTAIN CORRECT PC
6609 024222 001403          BEQ     3#           ; YES GO ON
6610                                     ; NO GO TO ERROR
6611 024224 104000          ERROR    ; ALL ERRORS TO TRAP TO EMT VECTOR
6612 024226 000654          .WORD   654           ; UNIQUE ERROR NUMBER
6613 024230 001127          .WORD   CPUERR        ; ADDRESS OF ERROR MESSAGE
6614 024232 022627 140000          3# : CMP      (SP)+,@#140000 ; DOES STACK CONTAIN CORRECT PSW
6615 024236 001403          BEQ     FIN120       ; YES GO ON
6616                                     ; NO GO TO ERROR
6617 024240 104000          ERROR    ; ALL ERRORS TO TRAP TO EMT VECTOR
6618 024242 000655          .WORD   655           ; UNIQUE ERROR NUMBER
6619 024244 001127          .WORD   CPUERR        ; ADDRESS OF ERROR MESSAGE
6620
6621 024246 005037 177766          FIN120: CLR      @#CPEREG ; CLEAR CPU ERROR REGISTER
6622 024252 012637 000006          MOV      (SP)+,@#6    ; RESTORE VECTOR
6623 024256 012637 000004          MOV      (SP)+,@#4    ; RESTORE VECTOR
6624
6625                                     ;
6626 024262          TE121:
6627                                     ; ;*****
6628                                     ; *TEST 206      TEST RESET
6629                                     ; ;*****
6630 024262          TST206:

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6743 024706 000002      8: RTI ;USER MODE HALT OCCURRED; GO TO ERROR.
6744
6745 024710 005037 177772      9: CLR 00177772 ;CLEAR PIRQ
6746 024714 005037 177776      CLR 00177776 ;CLEAR PSW
6747 024720 010237 000004      MOV R2,004 ;RESTORE VECTORS TO PREVIOUS STATE
6748 024724 010337 000006      MOV R3,006 ;
6749 024730
6750
6751
6752 024730
6753
6754
6755
6756 024730
6757 024730 005267 154050      TST207: INC 0TESTN ;INCREMENT TEST NUMBER
6758
6759 024734 012705 000010      MOV 08.,R5 ;INIT COUNTER
6760 024740 012701 025174      MOV 0T1220,R1 ;SETUP POINTER TO DATA
6761 024744 012737 030000 177776 1: MOV 030000,00177776 ;INIT PSW
6762 024752 004767 000064      JSR PC,T122A ; TEST INSTRUCTION
6763 024756 022137 177776      CMP (R1)+,00177776 ;IS PSW CORRECT
6764 024762 001403      BEQ 2: ;YES GO ON
6765 ;NO GO TO ERROR
6766 024764 104000      ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6767 024766 000671      .WORD 671 ;UNIQUE ERROR NUMBER
6768 024770 001127      .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6769
6770 024772 077514      2: SOB R5,1: ;REPEAT UNTIL ALL CASES ARE TESTED
6771
6772
6773 024774 012705 000010      MOV 08.,R5 ;INIT COUNTER
6774 025000 012737 140000 177776 3: MOV 0140000,00177776 ;SETUP PSW TO USER MODE
6775 025006 012706 000600      MOV 0600,R6 ;SETUP USER STACK
6776 025012 004767 000024      JSR PC,T122A ; TEST INSTRUCTION
6777 025016 022737 140017 177776      CMP 0140017,00177776 ;IS PSW CORRECT
6778 025024 001403      BEQ 4: ;YES GO ON
6779 ;NO GO TO ERROR
6780 025026 104000      ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
6781 025030 000672      .WORD 672 ;UNIQUE ERROR NUMBER
6782 025032 001127      .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
6783
6784 025034 077517      4: SOB R5,3: ;REPEAT UNTIL ALL CASES ARE TESTED
6785
6786
6787 025036 000167 000152      JMP FIN122
6788
6789 025042 020527 000010      T122A: CMP R5,08. ;FIND OUT WHAT COUNTER IS
6790 025046 001003      BNE 1: ;IF NOT PRIORITY 0 GO TO 1:
6791 025050 000277      SCC ;SET ALL CC BITS
6792 025052 000230      SPL 0 ;SET PRIORITY TO 0
6793 025054 000446      BR 8: ;RETURN
6794 025056 020527 000007 1: CMP R5,07 ;FIND OUT WHAT COUNTER IS
6795 025062 001003      BNE 2: ;IF NOT PRIORITY 1 GO TO 2:
6796 025064 000277      SCC ;SET ALL CC BITS
6797 025066 000231      SPL 1 ;SET PRIORITY TO 1
6798 025070 000440      BR 8: ;RETURN

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6799 025072 020527 000006      2#:  CMP      R5,#6      ;FIND OUT WHAT COUNTER IS
6800 025076 001003              BNE      3#           ;IF NOT PRIORITY 2 GO TO 3#
6801 025100 000277              SCC              ;SET ALL CC BITS
6802 025102 000232              SPL      2           ;SET PRIORITY TO 2
6803 025104 000432              BR       8#         ;RETURN
6804 025106 020527 000005      3#:  CMP      R5,#5      ;FIND OUT WHAT COUNTER IS
6805 025112 001003              BNE      4#         ;IF NOT PRIORITY 3 GO TO 4#
6806 025114 000277              SCC              ;SET ALL CC BITS
6807 025116 000233              SPL      3           ;SET PRIORITY TO 3
6808 025120 000424              BR       8#         ;RETURN
6809 025122 020527 000004      4#:  CMP      R5,#4      ;FIND OUT WHAT COUNTER IS
6810 025126 001003              BNE      5#         ;IF NOT PRIORITY 4 GO TO 5#
6811 025130 000277              SCC              ;SET ALL CC BITS
6812 025132 000234              SPL      4           ;SET PRIORITY TO 4
6813 025134 000416              BR       8#         ;RETURN
6814 025136 020527 000003      5#:  CMP      R5,#3      ;FIND OUT WHAT COUNTER IS
6815 025142 001003              BNE      6#         ;IF NOT PRIORITY 5 GO TO 6#
6816 025144 000277              SCC              ;SET ALL CC BITS
6817 025146 000235              SPL      5           ;SET PRIORITY TO 5
6818 025150 000410              BR       8#         ;RETURN
6819 025152 020527 000002      6#:  CMP      R5,#2      ;FIND OUT WHAT COUNTER IS
6820 025156 001003              BNE      7#         ;IF NOT PRIORITY 6 GO TO 7#
6821 025160 000277              SCC              ;SET ALL CC BITS
6822 025162 000236              SPL      6           ;SET PRIORITY TO 6
6823 025164 000402              BR       8#         ;RETURN
6824 025166 000277              7#:  SCC              ;SET ALL CC BITS
6825 025170 000237              SPL      7           ;SET PRIORITY TO 7
6826 025172 000207              8#:  RTS       PC      ;RETURN
6827
6828 025174 030017      T1228: .WORD    30017
6829 025176 030057      .WORD    30057
6830 025200 030117      .WORD    30117
6831 025202 030157      .WORD    30157
6832 025204 030217      .WORD    30217
6833 025206 030257      .WORD    30257
6834 025210 030317      .WORD    30317
6835 025212 030357      .WORD    30357
6836 025214
6837
6838 025214      FIN122:
6839
6840      TE123:
6841      ;*****
6842      ;*TEST 210      TEST TSTSET INSTRUCTION (MULTI PROCESSING INST)
6843      ;*****
6843 025214 005267 153564      TST210: INC      #TESTN      ;INCREMENT TEST NUMBER
6844 025220 005037 177776      CLR      @177776      ;INIT PSW
6845 025224 012703 000012      MOV      @10.,R3      ;INIT COUNTER
6846 025230 012701 000400      MOV      @400,R1      ;SETUP DESTINATION
6847 025234 012700 025426      MOV      @T123A,R0     ;SETUP SOURCE
6848 025240 012021      100#:  MOV      (R0)+,(R1)+   ;RELOCATE TABLES
6849 025242 077302      SOB      R3,100#      ;ARE WE DONE
6850 025244 013746 000010      MOV      @10,-(SP)    ;SAVE VECTOR
6851 025250 012737 025452 000010      MOV      @T123D,@#10  ;SETUP NEW VECTOR
6852 025256 005000      CLR      R0           ;INIT R0
6853 025260 012701 000400      MOV      @400,R1      ;SETUP POINTERS TO TABLES
6854 025264 012702 000410      MOV      @410,R2

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6855	025270	012703	000416			MOV	#416,R3		:
6856	025274	010104				MOV	R1,R4		:
6857	025276	012737	030000	177776	1#:	MOV	#30000,0#177776		: SETUP PSW
6858	025304	000262				SEV			: SET V BIT
6859	025306	007221				.WORD	7221		: TEST INSTRUCTION
6860	025310	022237	177776			CMP	(R2)+,0#177776		: IS PSW CORRECT
6861	025314	001403				BEQ	2#		: YES GO ON
6862									: NO GO TO ERROR
6863	025316	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
6864	025320	000673				.WORD	673		: UNIQUE ERROR NUMBER
6865	025322	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
6866									
6867	025324	020013			2#:	CMP	R0,(R3)		: IS R0 CORRECT
6868	025326	001403				BEQ	3#		: YES GO ON
6869									: NO GO TO ERROR
6870	025330	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
6871	025332	000674				.WORD	674		: UNIQUE ERROR NUMBER
6872	025334	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
6873									
6874	025336	005204			3#:	INC	R4		: SETUP EXPECTED DATA
6875	025340	005204				INC	R4		:
6876	025342	020401				CMP	R4,R1		: IS R1 CORRECT
6877	025344	001403				BEQ	4#		: YES GO ON
6878									: NO GO TO ERROR
6879	025346	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
6880	025350	000675				.WORD	675		: UNIQUE ERROR NUMBER
6881	025352	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
6882									
6883	025354	052713	000001		4#:	BIS	#1,(R3)		: SETUP EXPECTED DATA
6884	025360	022341				CMP	(R3)+,-(R1)		: IS TEST LOCATION CORRECT
6885	025362	001403				BEQ	5#		: YES GO ON
6886									: NO GO TO ERROR
6887	025364	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
6888	025366	000676				.WORD	676		: UNIQUE ERROR NUMBER
6889	025370	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
6890									
6891	025372	005201			5#:	INC	R1		: POINT TO NEXT TEST LOCATION
6892	025374	005201				INC	R1		:
6893	025376	021127	177777			CMP	(R1),#177777		: ARE WE DONE
6894	025402	001335				BNE	1#		: NO GO TO 1#
6895	025404	012737	025460	000010		MOV	#T123E,0#10		: SETUP NEW VECTOR
6896	025412	007201				.WORD	7201		: TEST INSTRUCTION ILLEGAL MODE
6897									: ERROR! GO TO ERROR IF DIDN'T TRAP
6898	025414	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
6899	025416	000677				.WORD	677		: UNIQUE ERROR NUMBER
6900	025420	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
6901									
6902	025422	000167	000036			JMP	T123F		
6903									
6904									
6905	025426	167604				T123A:	.WORD	167604	
6906	025430	000000					.WORD	0	
6907	025432	000001					.WORD	1	
6908	025434	177777					.WORD	177777	
6909	025436	030010			T123B:		.WORD	30010	
6910	025440	030004					.WORD	30004	


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6911 025442 030001
6912 025444 167604
6913 025446 000000
6914 025450 000001
6915
6916 025452
6917 025452 104000
6918 025454 000700
6919 025456 001127
6920
6921 025460 005726
6922 025462 005726
6923 025464 012637 000010
6924
6925
6926 025470
6927
6928
6929
6930 025470
6931 025470 005267 153310
6932 025474 005037 177776
6933 025500 012703 000012
6934 025504 012701 000400
6935 025510 012700 025714
6936 025514 012021
6937 025516 077302
6938 025520 013746 000010
6939 025524 012737 025740 000010
6940 025532 012701 000400
6941 025536 012702 000410
6942 025542 012703 000416
6943 025546 010204
6944 025550 012737 030000 177776 1$:
6945 025556 011100
6946 025560 020327 000416
6947 025564 001401
6948 025566 000402
6949 025570 000261 2$:
6950 025572 000401
6951 025574 000241 3$:
6952 025576 000262 4$:
6953 025600 007322
6954 025602 022337 177776
6955 025606 001403
6956
6957 025610 104000
6958 025612 000701
6959 025614 001127
6960
6961 025616 021100
6962 025620 001403
6963
6964 025622 104000
6965 025624 000702
6966 025626 001127

T123C: .WORD 30001
        .WORD 167604
        .WORD 0
        .WORD 1

T123D: ERROR
        .WORD 700
        .WORD CPUERR

T123E: TST (SP)+
        TST (SP)+
T123F: MOV (SP)+,0#10

;
TE124:
;*****
;*TEST 211 TEST WRTLCK (WRITE LOCK MULTI PROCESSING INST)
;*****
TST211:
        INC $TESTN ;INCREMENT TEST NUMBER
        CLR 0#177776 ;INIT PSW
        MOV #10,R3 ;INIT COUNTER
        MOV #400,R1 ;SETUP DESTINATION
        MOV #T124A,R0 ;SETUP SOURCE
100$: MOV (R0)+,(R1)+ ;RELOCATE TABLES
        SOB R3,100$ ;ARE WE DONE
        MOV 0#10,-(SP) ;SAVE VECTOR
        MOV #T124D,0#10 ;SETUP NEW VECTOR
        MOV #400,R1 ;SETUP POINTERS TO TABLES
        MOV #410,R2
        MOV #416,R3
        MOV R2,R4
        MOV #30000,0#177776 ;SETUP PSW
        MOV (R1),R0 ;SETUP R0
        CMP R3,#416 ;IS THIS THE FIRST TEST CASE
        BEQ 2$ ;YES GO TO 2$
        BR 3$ ;NO GO TO 3$
2$: SEC ;SET C BIT
        BR 4$
3$: CLC ;CLEAR C BIT
4$: SEV ;SET V BIT
        .WORD 7322 ; TEST INSTRUCTION
        CMP (R3)+,0#177776 ;IS PSW CORRECT
        BEQ 5$ ;YES GO ON
        ERROR! NO GO TO ERROR
        .WORD 701 ;ALL ERRORS TO TRAP TO EMT VECTOR
        .WORD CPUERR ;UNIQUE ERROR NUMBER
        ;ADDRESS OF ERROR MESSAGE

5$: CMP (R1),R0 ;IS R0 CORRECT
        BEQ 6$ ;YES GO ON
        ERROR! NO GO TO ERROR
        .WORD 702 ;ALL ERRORS TO TRAP TO EMT VECTOR
        .WORD CPUERR ;UNIQUE ERROR NUMBER
        ;ADDRESS OF ERROR MESSAGE

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7023 025756 005267 153022      INC      #TESTN      ;INCREMENT TEST NUMBER
7024 025762 005037 177776      CLR      @#177776    ;INIT PS
7025 025766 012701 026266      MOV      @TE125A,R1 ;SETUP POINTERS TO TABLES
7026
7027 025772 010137 001034      10:     MOV      R1,@#EXPDAT ;
7028 025776 062737 000002 001034      ADD      @2,@#EXPDAT ;POINT TO SOURCE
7029 026004 012703 122222      MOV      @122222,R3 ;INIT R3 TO A KNOWN STATE
7030 026010 011102      MOV      (R1),R2    ;INIT DESTINATION REG
7031 026012 000277      SCC      ;SET ALL CC BITS
7032 026014 070261 000002      MUL      2(R1),R2   ;TEST INSTRUCTION
7033 026020 026137 000004 177776      CMP      4(R1),@#177776 ;IS PS CORRECT
7034 026026 001403      BEQ      20         ;YES GO ON
7035
7036 026030 104000      ERROR   ;NO GO TO ERROR
7037 026032 000707      .WORD   707        ;ALL ERRORS TO TRAP TO EMT VECTOR
7038 026034 001127      .WORD   CPUERR     ;UNIQUE ERROR NUMBER
7039
7040 026036 026103 000006      20:     CMP      6(R1),R3   ;IS R3 CORRECT
7041 026042 001403      BEQ      30         ;YES GO ON
7042
7043 026044 104000      ERROR   ;NO GO TO ERROR
7044 026046 000710      .WORD   710        ;ALL ERRORS TO TRAP TO EMT VECTOR
7045 026050 001127      .WORD   CPUERR     ;UNIQUE ERROR NUMBER
7046
7047 026052 026102 000010      30:     CMP      10(R1),R2  ;IS R2 CORRECT
7048 026056 001403      BEQ      40         ;YES GO ON
7049
7050 026060 104000      ERROR   ;NO GO TO ERROR
7051 026062 000711      .WORD   711        ;ALL ERRORS TO TRAP TO EMT VECTOR
7052 026064 001127      .WORD   CPUERR     ;UNIQUE ERROR NUMBER
7053
7054 026066 026177 000002 152740 40:     CMP      2(R1),@#EXPDAT ;IS SOURCE LOCATION OK
7055 026074 001403      BEQ      50         ;YES GO ON
7056
7057 026076 104000      ERROR   ;NO GO TO ERROR
7058 026100 000712      .WORD   712        ;ALL ERRORS TO TRAP TO EMT VECTOR
7059 026102 001127      .WORD   CPUERR     ;UNIQUE ERROR NUMBER
7060
7061 026104 062701 000012      50:     ADD      @12,R1     ;GO TO NEXT TEST
7062 026110 020127 026514      CMP      R1,@#FIN125 ;ARE WE FINISHED
7063 026114 001326      BNE      10         ;NO GO TO 10
7064
7065
7066      ;SECOND PART
7067      ;USING ODD REGISTER
7068
7069 026116 012701 026266      60:     MOV      @TE125A,R1 ;SETUP POINTERS TO TABLES
7070 026122
7071
7072 026122 010102      MOV      R1,R2
7073 026124 012706 001000      MOV      @STBOT,R6 ;INIT R6 TO A KNOWN STATE
7074 026130 012704 000004      MOV      @4,R4      ;SETUP R4 VALUE
7075 026134 011105      MOV      (R1),R5    ;INIT DESTINATION REG
7076 026136 000277      SCC      ;SET ALL CC BITS
7077 026140 070561 000002      MUL      2(R1),R5   ;TEST INSTRUCTION
7078 026144 026137 000004 177776      CMP      4(R1),@#177776 ;IS PS CORRECT

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7135	026312	177777	.WORD	177777	;MULTIPLICAND
7136	026314	077777	.WORD	77777	;MULTIPLIER
7137	026316	000010	.WORD	10	
7138	026320	100001	.WORD	100001	
7139	026322	177777	.WORD	177777	
7140					
7141	026324	077777	.WORD	77777	;MULTIPLICAND
7142	026326	000456	.WORD	456	;MULTIPLIER
7143	026330	000001	.WORD	1	
7144	026332	177322	.WORD	177322	
7145	026334	000226	.WORD	226	
7146					
7147	026336	173210	.WORD	173210	;MULTIPLICAND
7148	026340	000000	.WORD	0	;MULTIPLIER
7149	026342	000004	.WORD	4	
7150	026344	000000	.WORD	0	
7151	026346	000000	.WORD	0	
7152					
7153	026350	000000	.WORD	0	;MULTIPLICAND
7154	026352	003251	.WORD	3251	;MULTIPLIER
7155	026354	000004	.WORD	4	
7156	026356	000000	.WORD	0	
7157	026360	000000	.WORD	0	
7158					
7159	026362	000000	.WORD	0	;MULTIPLICAND
7160	026364	000000	.WORD	0	;MULTIPLIER
7161	026366	000004	.WORD	4	
7162	026370	000000	.WORD	0	
7163	026372	000000	.WORD	0	
7164					
7165	026374	100000	.WORD	100000	;MULTIPLICAND
7166	026376	000001	.WORD	1	;MULTIPLIER
7167	026400	000010	.WORD	10	
7168	026402	100000	.WORD	100000	
7169	026404	177777	.WORD	177777	
7170					
7171	026406	077777	.WORD	77777	;MULTIPLICAND
7172	026410	000001	.WORD	1	;MULTIPLIER
7173	026412	000000	.WORD	0	
7174	026414	077777	.WORD	77777	
7175	026416	000000	.WORD	0	
7176					
7177	026420	000010	.WORD	10	;MULTIPLICAND
7178	026422	010000	.WORD	10000	;MULTIPLIER
7179	026424	000001	.WORD	1	
7180	026426	100000	.WORD	100000	
7181	026430	000000	.WORD	0	
7182					
7183	026432	001452	.WORD	1452	;MULTIPLICAND
7184	026434	034527	.WORD	34527	;MULTIPLIER
7185	026436	000001	.WORD	1	
7186	026440	066506	.WORD	66506	
7187	026442	000265	.WORD	265	
7188					
7189	026444	000007	.WORD	7	;MULTIPLICAND
7190	026446	000400	.WORD	400	;MULTIPLIER

7191	026450	000000				.WORD	0		
7192	026452	003400				.WORD	3400		
7193	026454	000000				.WORD	0		
7194									
7195	026456	000002				.WORD	2		;MULTIPLICAND
7196	026460	100000				.WORD	100000		;MULTIPLIER
7197	026462	000011				.WORD	11		
7198	026464	000000				.WORD	0		
7199	026466	177777				.WORD	177777		
7200									
7201	026470	100000				.WORD	100000		;MULTIPLICAND
7202	026472	077777				.WORD	77777		;MULTIPLIER
7203	026474	000011				.WORD	11		
7204	026476	100000				.WORD	100000		
7205	026500	140000				.WORD	140000		
7206									
7207	026502	000001				.WORD	1		;MULTIPLICAND
7208	026504	177777				.WORD	177777		;MULTIPLIER
7209	026506	000010				.WORD	10		
7210	026510	177777				.WORD	177777		
7211	026512	177777				.WORD	177777		
7212	026514								
7213									
7214	026514								
7215									
7216									
7217									
7218	026514								
7219	026514	005267	152264			INC	#TESTN		;INCREMENT TEST NUMBER
7220	026520	005037	177776			CLR	#0177776		;INIT PSW
7221	026524	005006				CLR	R6		;INIT SP
7222	026526	013705	000000			MOV	#0,R5		;SAVE VECTORS
7223	026532	013701	000002			MOV	#02,R1		
7224	026536	012737	000137	000000		MOV	#137,#00		;SETUP NEW VECTORS
7225	026544	012737	026572	000002		MOV	#TE126A,#02		
7226	026552	000277				SCC			
7227	026554	071627	000002			DIV	#2,R6		;SET ALL CC BITS
7228	026560	012706	001000		A126:	MOV	#STBOT,R6		; TEST INSTRUCTION
7229									;RESTORE SP BEFORE GOING TO ERROR
7230	026564	104000				ERROR			;IF R7 ISN'T CORRECT GO TO ERROR
7231	026566	000720				.WORD	720		;ALL ERRORS TO TRAP TO EMT VECTOR
7232	026570	001127				.WORD	CPUERR		;UNIQUE ERROR NUMBER
7233									;ADDRESS OF ERROR MESSAGE
7234	026572	022737	000000	177776	TE126A:	CMP	#0,#0177776		;IS PS CORRECT
7235	026600	001405				BEQ	1#		;YES GO ON
7236	026602	012706	001000			MOV	#STBOT,R6		;RESTORE SP BEFORE GOING TO ERROR
7237									;NO GO TO ERROR
7238	026606	104000				ERROR			;ALL ERRORS TO TRAP TO EMT VECTOR
7239	026610	000721				.WORD	721		;UNIQUE ERROR NUMBER
7240	026612	001127				.WORD	CPUERR		;ADDRESS OF ERROR MESSAGE
7241									
7242	026614	012704	026560		1#:	MOV	#A126,R4		;SETUP EXPECTED DATA
7243	026620	006204				ASR	R4		
7244	026622	020406				CMP	R4,R6		;IS R6 CORRECT
7245	026624	001405				BEQ	2#		;YES GO ON
7246	026626	012706	001000			MOV	#STBOT,R6		;RESTORE SP BEFORE GOING TO ERROR


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7415 027360 001316          BNE      16#          ;NO GO TO 16#
7416
7417
7418 027362 000167 000316          JMP      FIN126
7419
7420
7421      ;
7421      ;TE126B: .WORD 177777 ;DIVIDEND
7422      .WORD 177777 ;INIT R5
7423      .WORD 177777 ;DIVISOR
7424      .WORD 0 ;PSW
7425      .WORD 0 ;R5 RESULT
7426      .WORD 1 ;R4 RESULT
7427
7428      .WORD 0 ;DIVIDEND
7429      .WORD 177777 ;INIT R5
7430      .WORD 177777 ;DIVISOR
7431      .WORD 12 ;PSW
7432      .WORD 177777 ;R5 RESULT
7433      .WORD 0 ;R4 RESULT
7434
7435      .WORD 177777 ;DIVIDEND
7436      .WORD 0 ;INIT R5
7437      .WORD 177777 ;DIVISOR
7438      .WORD 2 ;PSW
7439      .WORD 0 ;R5 RESULT
7440      .WORD 177777 ;R4 RESULT
7441
7442      .WORD 0 ;DIVIDEND
7443      .WORD 7642 ;INIT R5
7444      .WORD 7643 ;DIVISOR
7445      .WORD 4 ;PSW
7446      .WORD 7642 ;R5 RESULT
7447      .WORD 0 ;R4 RESULT
7448
7449      .WORD 0 ;DIVIDEND
7450      .WORD 137 ;INIT R5
7451      .WORD 177543 ;DIVISOR
7452      .WORD 4 ;PSW
7453      .WORD 137 ;R5 RESULT
7454      .WORD 0 ;R4 RESULT
7455
7456      .WORD 0 ;DIVIDEND
7457      .WORD 7643 ;INIT R5
7458      .WORD 7643 ;DIVISOR
7459      .WORD 0 ;PSW
7460      .WORD 0 ;R5 RESULT
7461      .WORD 1 ;R4 RESULT
7462
7463      .WORD 100000 ;DIVIDEND
7464      .WORD 4376 ;INIT R5
7465      .WORD 10021 ;DIVISOR
7466      .WORD 12 ;PSW
7467      .WORD 4376 ;R5 RESULT
7468      .WORD 100000 ;R4 RESULT
7469
7470      .WORD 177700 ;DIVIDEND
    
```


7471	027514	170033	.WORD	170033	:INIT R5
7472	027516	010021	.WORD	10021	:DIVISOR
7473	027520	000010	.WORD	10	:PSW
7474	027522	171307	.WORD	171307	:R5 RESULT
7475	027524	176024	.WORD	176024	:R4 RESULT
7476					
7477	027526	177700	.WORD	177700	:DIVIDEND
7478	027530	170033	.WORD	170033	:INIT R5
7479	027532	167757	.WORD	167757	:DIVISOR
7480	027534	000000	.WORD	0	:PSW
7481	027536	171307	.WORD	171307	:R5 RESULT
7482	027540	001754	.WORD	1754	:R4 RESULT
7483					
7484	027542	000000	.WORD	0	:DIVIDEND
7485	027544	177777	.WORD	177777	:INIT R5
7486	027546	000001	.WORD	1	:DIVISOR
7487	027550	000002	.WORD	2	:PSW
7488	027552	177777	.WORD	177777	:R5 RESULT
7489	027554	000000	.WORD	0	:R4 RESULT
7490					
7491	027556	177777	.WORD	177777	:DIVIDEND
7492	027560	045716	.WORD	45716	:INIT R5
7493	027562	000001	.WORD	1	:DIVISOR
7494	027564	000012	.WORD	12	:PSW
7495	027566	045716	.WORD	45716	:R5 RESULT
7496	027570	177777	.WORD	177777	:R4 RESULT
7497					
7498	027572	000000	.WORD	0	:DIVIDEND
7499	027574	000002	.WORD	2	:INIT R5
7500	027576	177770	.WORD	177770	:DIVISOR
7501	027600	000004	.WORD	4	:PSW
7502	027602	000002	.WORD	2	:R5 RESULT
7503	027604	000000	.WORD	0	:R4 RESULT
7504					
7505	027606	177777	.WORD	177777	:DIVIDEND
7506	027610	177776	.WORD	177776	:INIT R5
7507	027612	000010	.WORD	10	:DIVISOR
7508	027614	000004	.WORD	4	:PSW
7509	027616	177776	.WORD	177776	:R5 RESULT
7510	027620	000000	.WORD	0	:R4 RESULT
7511					
7512	027622	000001	.WORD	1	:DIVIDEND
7513	027624	177777	.WORD	177777	:INIT R5
7514	027626	000001	.WORD	1	:DIVISOR
7515	027630	000002	.WORD	2	:PSW
7516	027632	177777	.WORD	177777	:R5 RESULT
7517	027634	000001	.WORD	1	:R4 RESULT
7518					
7519	027636	000001	.WORD	1	:DIVIDEND
7520	027640	000000	.WORD	0	:INIT R5
7521	027642	000002	.WORD	2	:DIVISOR
7522	027644	000002	.WORD	2	:PSW
7523	027646	000000	.WORD	0	:R5 RESULT
7524	027650	000001	.WORD	1	:R4 RESULT
7525					
7526	027652	000001	.WORD	1	:DIVIDEND

7527	027654	000000			.WORD	0		;INIT R5
7528	027656	000003			.WORD	3		;DIVISOR
7529	027660	000000			.WORD	0		;PSW
7530	027662	000001			.WORD	1		;R5 RESULT
7531	027664	052525			.WORD	52525		;R4 RESULT
7532								
7533	027666	000023			.WORD	23		;DIVIDEND
7534	027670	016054			.WORD	16054		;INIT R5
7535	027672	016537			.WORD	16537		;DIVISOR
7536	027674	000000			.WORD	0		;PSW
7537	027676	010222			.WORD	10222		;R5 RESULT
7538	027700	000246			.WORD	246		;R4 RESULT
7539								
7540	027702	000333			.WORD	333		
7541	027704							
7542								
7543	027704							
7544								
7545								
7546								
7547	027704							
7548	027704	005267	151074					
7549	027710	005037	177776					
7550	027714	012702	000001					
7551	027720	000277						
7552	027722	072202						
7553	027724	022737	000000	177776				
7554	027732	001403						
7555								
7556	027734	104000						
7557	027736	000745						
7558	027740	001127						
7559								
7560	027742	020227	000002					
7561	027746	001403						
7562								
7563	027750	104000						
7564	027752	000746						
7565	027754	001127						
7566								
7567	027756	012702	100000					
7568	027762	012703	000001					
7569	027766	000257						
7570	027770	072203						
7571	027772	022737	000007	177776				
7572	030000	001403						
7573								
7574	030002	104000						
7575	030004	000747						
7576	030006	001127						
7577								
7578	030010	020327	000001					
7579	030014	001403						
7580								
7581	030016	104000						
7582	030020	000750						

FIN126:

TE127:

:TEST 214 TEST ASH (ARITHMETIC SHIFT)

TST214:

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INC      #TESTN      ;INCREMENT TEST NUMBER
CLR      #0177776    ;INIT PSW
MOV      #1,R2       ;SETUP OPERAND
SCC      ;SET ALL CC BITS
ASH      R2,R2       ; TEST INSTRUCTION
CMP      #0,#0177776 ;IS PS CORRECT
BEQ      1#          ;YES GO ON
                     ;NO GO TO ERROR
                     ;ALL ERRORS TO TRAP TO EMT VECTOR
ERROR    745         ;UNIQUE ERROR NUMBER
.WORD    CPUERR      ;ADDRESS OF ERROR MESSAGE

1# :    CMP      R2,#2 ;IS R2 CORRECT
        BEQ      2#   ;YES GO ON
                     ;NO GO TO ERROR
                     ;ALL ERRORS TO TRAP TO EMT VECTOR
ERROR    746         ;UNIQUE ERROR NUMBER
.WORD    CPUERR      ;ADDRESS OF ERROR MESSAGE

2# :    MOV      #100000,R2 ;SETUP R2
        MOV      #1,R3     ;SETUP R3
        CCC      ;CLEAR ALL CC BITS
        ASH      R3,R2     ; TEST INSTRUCTION
        CMP      #7,#0177776 ;IS PS CORRECT
        BEQ      3#       ;YES GO ON
                     ;NO GO TO ERROR
                     ;ALL ERRORS TO TRAP TO EMT VECTOR
ERROR    747         ;UNIQUE ERROR NUMBER
.WORD    CPUERR      ;ADDRESS OF ERROR MESSAGE

3# :    CMP      R3,#1     ;IS R3 CORRECT
        BEQ      4#       ;YES GO ON
                     ;NO GO TO ERROR
                     ;ALL ERRORS TO TRAP TO EMT VECTOR
ERROR    750         ;UNIQUE ERROR NUMBER
.WORD    CPUERR      ;ADDRESS OF ERROR MESSAGE

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7583	030022	001127			.WORD	CPUERR			;ADDRESS OF ERROR MESSAGE
7584									
7585	030024	020227	000000	4#:	CMP	R2,#0			;IS R2 CORRECT
7586	030030	001403			BEQ	5#			;YES GO ON
7587									;NO GO TO ERROR
7588	030032	104000			ERROR				;ALL ERRORS TO TRAP TO EMT VECTOR
7589	030034	000751			.WORD	751			;UNIQUE ERROR NUMBER
7590	030036	001127			.WORD	CPUERR			;ADDRESS OF ERROR MESSAGE
7591									
7592	030040	012701	030154	5#:	MOV	#TE127A,R1			;SETUP POINTERS TO TABLES
7593									
7594	030044	010103		6#:	MOV	R1,R3			;SETUP R2
7595	030046	016102	000002		MOV	2(R1),R2			;SET ALL CC BITS
7596	030052	000277			SCC				;TEST INSTRUCTION
7597	030054	072211			ASH	(R1),R2			;IS PS CORRECT
7598	030056	026137	000004	177776	CMP	4(R1),#0177776			;YES GO ON
7599	030064	001403			BEQ	7#			;NO GO TO ERROR
7600									;ALL ERRORS TO TRAP TO EMT VECTOR
7601	030066	104000			ERROR				;UNIQUE ERROR NUMBER
7602	030070	000752			.WORD	752			;ADDRESS OF ERROR MESSAGE
7603	030072	001127			.WORD	CPUERR			
7604									
7605	030074	026102	000006	7#:	CMP	6(R1),R2			;IS R2 CORRECT
7606	030100	001403			BEQ	8#			;YES GO ON
7607									;NO GO TO ERROR
7608	030102	104000			ERROR				;ALL ERRORS TO TRAP TO EMT VECTOR
7609	030104	000753			.WORD	753			;UNIQUE ERROR NUMBER
7610	030106	001127			.WORD	CPUERR			;ADDRESS OF ERROR MESSAGE
7611									
7612	030110	020301		8#:	CMP	R3,R1			;IS R1 CORRECT
7613	030112	001404			BEQ	9#			;YES GO ON
7614									;NO GO TO ERROR
7615	030114	104000			ERROR				;ALL ERRORS TO TRAP TO EMT VECTOR
7616	030116	000754			.WORD	754			;UNIQUE ERROR NUMBER
7617	030120	001127			.WORD	CPUERR			;ADDRESS OF ERROR MESSAGE
7618	030122	010301			MOV	R3,R1			;RESTORE R1
7619									
7620	030124	021311		9#:	CMP	(R3),(R1)			;IS SOURCE CORRECT
7621	030126	001403			BEQ	10#			;YES GO ON
7622									;NO GO TO ERROR
7623	030130	104000			ERROR				;ALL ERRORS TO TRAP TO EMT VECTOR
7624	030132	000755			.WORD	755			;UNIQUE ERROR NUMBER
7625	030134	001127			.WORD	CPUERR			;ADDRESS OF ERROR MESSAGE
7626									;SOURCE LOOKS INCORRECT
7627	030136	062701	000010	10#:	ADD	#10,R1			;INCREMENT POINTER
7628	030142	020127	030414		CMP	R1,#FIN127			;ARE WE DONE
7629	030146	001336			BNE	6#			;NO GO TO 6#
7630									
7631									
7632	030150	000167	000240		JMP	FIN127			
7633									
7634									
7635	030154	177761			.WORD	177761			;SOURCE
7636	030156	077777			.WORD	77777			;DEST
7637	030160	000005			.WORD	5			
7638	030162	000000			.WORD	0			

7639					
7640	030164	177700	.WORD	177700	;SOURCE
7641	030166	017777	.WORD	17777	;DEST
7642	030170	000000	.WORD	0	
7643	030172	017777	.WORD	17777	
7644					
7645	030174	177700	.WORD	177700	;SOURCE
7646	030176	100000	.WORD	100000	;DEST
7647	030200	000010	.WORD	10	
7648	030202	100000	.WORD	100000	
7649					
7650	030204	177777	.WORD	177777	;SOURCE
7651	030206	100000	.WORD	100000	;DEST
7652	030210	000010	.WORD	10	
7653	030212	140000	.WORD	140000	
7654					
7655	030214	177737	.WORD	177737	;SOURCE
7656	030216	177777	.WORD	177777	;DEST
7657	030220	000011	.WORD	11	
7658	030222	177777	.WORD	177777	
7659					
7660	030224	177706	.WORD	177706	;SOURCE
7661	030226	102000	.WORD	102000	;DEST
7662	030230	000007	.WORD	7	
7663	030232	000000	.WORD	0	
7664					
7665	030234	177710	.WORD	177710	;SOURCE
7666	030236	017777	.WORD	17777	;DEST
7667	030240	000013	.WORD	13	
7668	030242	177400	.WORD	177400	
7669					
7670	030244	177713	.WORD	177713	;SOURCE
7671	030246	000012	.WORD	12	;DEST
7672	030250	000000	.WORD	0	
7673	030252	050000	.WORD	50000	
7674					
7675	030254	177707	.WORD	177707	;SOURCE
7676	030256	170001	.WORD	170001	;DEST
7677	030260	000002	.WORD	2	
7678	030262	000200	.WORD	200	
7679					
7680	030264	177717	.WORD	177717	;SOURCE
7681	030266	000001	.WORD	1	;DEST
7682	030270	000012	.WORD	12	
7683	030272	100000	.WORD	100000	
7684					
7685	030274	177740	.WORD	177740	;SOURCE
7686	030276	017777	.WORD	17777	;DEST
7687	030300	000004	.WORD	4	
7688	030302	000000	.WORD	0	
7689					
7690	030304	177771	.WORD	177771	;SOURCE
7691	030306	150000	.WORD	150000	;DEST
7692	030310	000010	.WORD	10	
7693	030312	177640	.WORD	177640	
7694					

7695	030314	177742	.WORD	177742	;SOURCE
7696	030316	100000	.WORD	100000	;DEST
7697	030320	000011	.WORD	11	
7698	030322	177777	.WORD	177777	
7699					
7700	030324	177764	.WORD	177764	;SOURCE
7701	030326	100000	.WORD	100000	;DEST
7702	030330	000010	.WORD	10	
7703	030332	177770	.WORD	177770	
7704					
7705	030334	177750	.WORD	177750	;SOURCE
7706	030336	052525	.WORD	52525	;DEST
7707	030340	000004	.WORD	4	
7708	030342	000000	.WORD	0	
7709					
7710	030344	177760	.WORD	177760	;SOURCE
7711	030346	100000	.WORD	100000	;DEST
7712	030350	000011	.WORD	11	
7713	030352	177777	.WORD	177777	
7714					
7715	030354	177770	.WORD	177770	;SOURCE
7716	030356	100000	.WORD	100000	;DEST
7717	030360	000010	.WORD	10	
7718	030362	177600	.WORD	177600	
7719					
7720	030364	177712	.WORD	177712	;SOURCE
7721	030366	004367	.WORD	4367	;DEST
7722	030370	000013	.WORD	13	
7723	030372	156000	.WORD	156000	
7724					
7725	030374	177764	.WORD	177764	;SOURCE
7726	030376	017777	.WORD	17777	;DEST
7727	030400	000001	.WORD	1	
7728	030402	000001	.WORD	1	
7729					
7730	030404	177701	.WORD	177701	;SOURCE
7731	030406	110000	.WORD	110000	;DEST
7732	030410	000003	.WORD	3	
7733	030412	020000	.WORD	20000	
7734					

FIN127:

;TE130:

;;*****

;+TEST 215 TEST ASHC (ARITHMETIC SHIFT COMBINED)

;;*****

```

TST215:
INC      ;TESTN      ;INCREMENT TEST NUMBER
CLR      ;0177776    ;INIT PSW
MOV      ;R1         ;SETUP R1
MOV      ;R5,R5     ;SETUP R5
CLR      ;R4         ;SETUP R4
SCC      ;          ;SET ALL CC BITS
ASHC     ;R1,R4     ;TEST INSTRUCTION
CMP      ;0177776,012 ;IS PS CORRECT
BEQ      ;          ;YES GO ON

```

7741	030414				
7742	030414	005267	150364		
7743	030420	005037	177776		
7744	030424	012701	000023		
7745	030430	012705	052525		
7746	030434	005004			
7747	030436	000277			
7748	030440	073401			
7749	030442	023727	177776	000012	
7750	030450	001403			

7863	030764	100125	.WORD	100125	:DESTINATION WORD 1
7864	030766	177777	.WORD	177777	:DESTINATION WORD 2
7865	030770	000010	.WORD	10	:TEST PSW
7866	030772	100125	.WORD	100125	:RESULT WORD 1
7867	030774	177777	.WORD	177777	:RESULT WORD 2
7868					
7869	030776	177777	.WORD	177777	:SOURCE
7870	031000	000001	.WORD	1	:DESTINATION WORD 1
7871	031002	000000	.WORD	0	:DESTINATION WORD 2
7872	031004	000000	.WORD	0	:TEST PSW
7873	031006	000000	.WORD	0	:RESULT WORD 1
7874	031010	100000	.WORD	100000	:RESULT WORD 2
7875					
7876	031012	177701	.WORD	177701	:SOURCE
7877	031014	047777	.WORD	47777	:DESTINATION WORD 1
7878	031016	100000	.WORD	100000	:DESTINATION WORD 2
7879	031020	000012	.WORD	12	:TEST PSW
7880	031022	117777	.WORD	117777	:RESULT WORD 1
7881	031024	000000	.WORD	0	:RESULT WORD 2
7882					
7883	031026	177706	.WORD	177706	:SOURCE
7884	031030	004256	.WORD	4256	:DESTINATION WORD 1
7885	031032	177700	.WORD	177700	:DESTINATION WORD 2
7886	031034	000002	.WORD	2	:TEST PSW
7887	031036	025677	.WORD	25677	:RESULT WORD 1
7888	031040	170000	.WORD	170000	:RESULT WORD 2
7889					
7890	031042	177711	.WORD	177711	:SOURCE
7891	031044	065700	.WORD	65700	:DESTINATION WORD 1
7892	031046	000012	.WORD	12	:DESTINATION WORD 2
7893	031050	000013	.WORD	13	:TEST PSW
7894	031052	100000	.WORD	100000	:RESULT WORD 1
7895	031054	012000	.WORD	12000	:RESULT WORD 2
7896					
7897	031056	177737	.WORD	177737	:SOURCE
7898	031060	000000	.WORD	0	:DESTINATION WORD 1
7899	031062	000001	.WORD	1	:DESTINATION WORD 2
7900	031064	000004	.WORD	4	:TEST PSW
7901	031066	000000	.WORD	0	:RESULT WORD 1
7902	031070	000000	.WORD	0	:RESULT WORD 2
7903					
7904	031072	177736	.WORD	177736	:SOURCE
7905	031074	000000	.WORD	0	:DESTINATION WORD 1
7906	031076	000001	.WORD	1	:DESTINATION WORD 2
7907	031100	000000	.WORD	0	:TEST PSW
7908	031102	040000	.WORD	40000	:RESULT WORD 1
7909	031104	000000	.WORD	0	:RESULT WORD 2
7910					
7911	031106	177740	.WORD	177740	:SOURCE
7912	031110	100000	.WORD	100000	:DESTINATION WORD 1
7913	031112	000000	.WORD	0	:DESTINATION WORD 2
7914	031114	000011	.WORD	11	:TEST PSW
7915	031116	177777	.WORD	177777	:RESULT WORD 1
7916	031120	177777	.WORD	177777	:RESULT WORD 2
7917					
7918	031122	177725	.WORD	177725	:SOURCE

7919	031124	177777	.WORD	177777	;DESTINATION WORD 1
7920	031126	174000	.WORD	174000	;DESTINATION WORD 2
7921	031130	000007	.WORD	7	;TEST PSW
7922	031132	000000	.WORD	0	;RESULT WORD 1
7923	031134	000000	.WORD	0	;RESULT WORD 2
7924					
7925	031136	177724	.WORD	177724	;SOURCE
7926	031140	177777	.WORD	177777	;DESTINATION WORD 1
7927	031142	174000	.WORD	174000	;DESTINATION WORD 2
7928	031144	000011	.WORD	11	;TEST PSW
7929	031146	100000	.WORD	100000	;RESULT WORD 1
7930	031150	000000	.WORD	0	;RESULT WORD 2
7931					
7932	031152	177733	.WORD	177733	;SOURCE
7933	031154	177777	.WORD	177777	;DESTINATION WORD 1
7934	031156	157023	.WORD	157023	;DESTINATION WORD 2
7935	031160	000012	.WORD	12	;TEST PSW
7936	031162	114000	.WORD	114000	;RESULT WORD 1
7937	031164	000000	.WORD	0	;RESULT WORD 2
7938					
7939	031166	177727	.WORD	177727	;SOURCE
7940	031170	000000	.WORD	0	;DESTINATION WORD 1
7941	031172	177777	.WORD	177777	;DESTINATION WORD 2
7942	031174	000013	.WORD	13	;TEST PSW
7943	031176	177600	.WORD	177600	;RESULT WORD 1
7944	031200	000000	.WORD	0	;RESULT WORD 2
7945					
7946	031202	177717	.WORD	177717	;SOURCE
7947	031204	177777	.WORD	177777	;DESTINATION WORD 1
7948	031206	000001	.WORD	1	;DESTINATION WORD 2
7949	031210	000011	.WORD	11	;TEST PSW
7950	031212	100000	.WORD	100000	;RESULT WORD 1
7951	031214	100000	.WORD	100000	;RESULT WORD 2
7952					
7953	031216	177741	.WORD	177741	;SOURCE
7954	031220	100000	.WORD	100000	;DESTINATION WORD 1
7955	031222	000000	.WORD	0	;DESTINATION WORD 2
7956	031224	000010	.WORD	10	;TEST PSW
7957	031226	177777	.WORD	177777	;RESULT WORD 1
7958	031230	177777	.WORD	177777	;RESULT WORD 2
7959					
7960	031232	177742	.WORD	177742	;SOURCE
7961	031234	037777	.WORD	37777	;DESTINATION WORD 1
7962	031236	177777	.WORD	177777	;DESTINATION WORD 2
7963	031240	000005	.WORD	5	;TEST PSW
7964	031242	000000	.WORD	0	;RESULT WORD 1
7965	031244	000000	.WORD	0	;RESULT WORD 2
7966					
7967	031246	177742	.WORD	177742	;SOURCE
7968	031250	077777	.WORD	77777	;DESTINATION WORD 1
7969	031252	177777	.WORD	177777	;DESTINATION WORD 2
7970	031254	000001	.WORD	1	;TEST PSW
7971	031256	000000	.WORD	0	;RESULT WORD 1
7972	031260	000001	.WORD	1	;RESULT WORD 2
7973					
7974	031262	177711	.WORD	177711	;SOURCE

7975	031264	065600	.WORD	65600	;DESTINATION WORD 1
7976	031266	000012	.WORD	12	;DESTINATION WORD 2
7977	031270	000003	.WORD	3	;TEST PSW
7978	031272	000000	.WORD	0	;RESULT WORD 1
7979	031274	012000	.WORD	12000	;RESULT WORD 2
7980					
7981	031276	177740	.WORD	177740	;SOURCE
7982	031300	077777	.WORD	77777	;DESTINATION WORD 1
7983	031302	177777	.WORD	177777	;DESTINATION WORD 2
7984	03_304	000004	.WORD	4	;TEST PSW
7985	031306	000000	.WORD	0	;RESULT WORD 1
7986	031310	000000	.WORD	0	;RESULT WORD 2
7987					
7988	031312	177737	.WORD	177737	;SOURCE
7989	031314	177777	.WORD	177777	;DESTINATION WORD 1
7990	031316	177774	.WORD	177774	;DESTINATION WORD 2
7991	031320	000011	.WORD	11	;TEST PSW
7992	031322	177777	.WORD	177777	;RESULT WORD 1
7993	031324	177777	.WORD	177777	;RESULT WORD 2
7994					
7995	031326	177747	.WORD	177747	;SOURCE
7996	031330	100000	.WORD	100000	;DESTINATION WORD 1
7997	031332	174000	.WORD	174000	;DESTINATION WORD 2
7998	031334	000010	.WORD	10	;TEST PSW
7999	031336	177777	.WORD	177777	;RESULT WORD 1
8000	031340	177700	.WORD	177700	;RESULT WORD 2
8001					
8002	031342	177753	.WORD	177753	;SOURCE
8003	031344	006324	.WORD	6324	;DESTINATION WORD 1
8004	031346	071002	.WORD	71002	;DESTINATION WORD 2
8005	031350	000001	.WORD	1	;TEST PSW
8006	031352	000000	.WORD	0	;RESULT WORD 1
8007	031354	000146	.WORD	146	;RESULT WORD 2
8008					
8009	031356	177765	.WORD	177765	;SOURCE
8010	031360	102351	.WORD	102351	;DESTINATION WORD 1
8011	031362	177231	.WORD	177231	;DESTINATION WORD 2
8012	031364	000011	.WORD	11	;TEST PSW
8013	031366	177760	.WORD	177760	;RESULT WORD 1
8014	031370	116477	.WORD	116477	;RESULT WORD 2
8015	031372				
8016	031372				
8017					
8018					
8019					
8020	031372				
8021	031372	005267	147406		
8022	031376	005006			
8023	031400	112667	147434		
8024	031404	022706	000002		
8025	031410	001403			
8026					
8027	031412	104000			
8028	031414	000773			
8029	031416	001127			
8030	031420	005006			

```

FIN130:
MSPAU:
;*****
;*TEST 216      TEST THAT AUTO DEC/INC OPERATIONS USING SP ARE ON WORD BOUNDARYS
;*****
TST216:
      INC      ;TESTN
      CLR      R6
      MOVB     (R6)+,COUNT
      CMP      #2,R6
      BEQ      SPAU1
      ERROR
      .WORD    773
      .WORD    CPUERR
SPAU1:  CLR      R6
;INCREMENT TEST NUMBER
;CLEAR SP
;TRY AUTOINC ON R6
;VERIFY AUTO INC BY 2
;BRANCH IF GOOD
;BAD AUTO-INC
;ALL ERRORS TO TRAP TO EMT VECTOR
;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE
;CLEAR R6

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8031 031422 112667 147412      MOVB      (R6)+,COUNT
8032 031426 112667 147406      MOVB      (R6)+,COUNT      ;DOUBLE BYTE AUTO-INC
8033 031432 022706 000004      CMP       #4,R6             ;VERIFY RESULT
8034 031436 001403              BEQ       SPAU2             ;BRANCH IF GOOD
8035                                ;BAD DOUBLE AUTO-INC
8036 031440 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
8037 031442 000774              .WORD    774                ;UNIQUE ERROR NUMBER
8038 031444 001127              .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
8039 031446 012706 001000      SPAU2:  MOV     #STBOT,R6     ;LOAD R6
8040 031452 114667 147362      MOVB     -(R6),COUNT      ; TEST AUTO-DEC
8041 031456 022706 000776      CMP      #776,R6          ;VERIFY RESULT
8042 031462 001403              BEQ      SPAU3             ;BRANCH IF GOOD
8043 031464 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
8044 031466 000775              .WORD    775                ;UNIQUE ERROR NUMBER
8045 031470 001127              .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
8046 031472 012706 001000      SPAU3:  MOV     #STBOT,R6     ;LOAD R6
8047 031476 114667 147336      MOVB     -(R6),COUNT      ; TEST AUTO-DEC
8048 031502 114667 147332      MOVB     -(R6),COUNT      ; TEST AUTO-DEC
8049 031506 022706 000774      CMP      #774,R6          ;VERIFY RESULT
8050 031512 001403              BEQ      SPAU4             ;BRANCH IF GOOD
8051 031514 104000              ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
8052 031516 000776              .WORD    776                ;UNIQUE ERROR NUMBER
8053 031520 001127              .WORD    CPUERR             ;ADDRESS OF ERROR MESSAGE
8054 031522 005006      SPAU4:  CLR      R6             ; TEST AUTO-INC ON SOP
8055 031524 105726              TSTB     (R6)+            ; TEST AUTO-INC
8056 031526 020627 000002      CMP      R6,#2            ;BRANCH IF GOOD
8057 031532 001403              BEQ      SPAU5             ;ALL ERRORS TO TRAP TO EMT VECTOR
8058 031534 104000              ERROR                                ;UNIQUE ERROR NUMBER
8059 031536 000777              .WORD    777                ;ADDRESS OF ERROR MESSAGE
8060 031540 001127              .WORD    CPUERR             ;LOAD R6
8061 031542 012706 001000      SPAU5:  MOV     #STBOT,R6     ; TEST AUTO-DEC
8062 031546 105746              TSTB     -(R6)            ;VERIFY RESULT
8063 031550 022706 000776      CMP      #776,R6          ;BRANCH IF GOOD
8064 031554 001403              BEQ      SPAU6             ;ALL ERRORS TO TRAP TO EMT VECTOR
8065 031556 104000              ERROR                                ;UNIQUE ERROR NUMBER
8066 031560 001000              .WORD    1000              ;ADDRESS OF ERROR MESSAGE
8067 031562 001127              .WORD    CPUERR
8068 031564 012706 001000      SPAU6:  MOV     #STBOT,R6
8069
8070
8071 031570      ;
8072      ;*****
8073      ;*TEST 217      VERIFY YELLOW ZONE TRAP ON AUTO DEC OF R6
8074      ;*****
8075 031570      TST217:
8076 031570 005267 147210      INC      #TESTN            ;INCREMENT TEST NUMBER
8077 031574 005067 146166      CLR      CPEREG           ;INIT CPU ERROR REGISTER
8078 031600 012706 000150      MOV     #150,R6           ;LOAD R6 WITH A VALUE THAT WILL
8079                                ;CAUSE A YELLOW STACK TRAP(IE. <400)
8080 031604 016767 146174 147216      MOV     4,SLOC00          ;SAVE VECTOR
8081 031612 012767 031654 146164      MOV     #MTRYA,4         ;SETUP THE STACK OVERFLOW TRAP POINTER
8082 031620 016701 146322      MOV     146,R1            ;SAVE VECTOR
8083 031624 016702 146314      MOV     144,R2            ;SAVE VECTOR
8084 031630 016703 146306      MOV     142,R3            ;SAVE VECTOR
8085 031634 005067 146306      CLR     146               ;JUST AS A PRECAUTION
8086 031640 005046              CLR     -(R6)            ;CAUSE A STACK OVERFLOW TRAP

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8087 031642 012706 001000      MOV      #STBOT,R6      ;RESTORE R6 FOR ERROR CALL
8088                                ;OVERFLOW TRAP FAILED
8089                                ;ALL ERRORS TO TRAP TO EMT VECTOR
8090 031646 104000      ERROR                                ;UNIQUE ERROR NUMBER
8091 031650 001001      .WORD 1001                                ;ADDRESS OF ERROR MESSAGE
8092 031652 001127      .WORD CPUERR
8093 031654 022767 000010 146104 MTRYA:  CMP      #BIT03,CPEREG  ;WAS CPU ERROR REG SET PROPERLY?
8094 031662 001003      BNE     1#                                ;GO TO ERROR IF NOT
8095 031664 020627 000142      CMP      R6,#142      ;VERIFY CORRECT DECREMENT OF R6
8096 031670 001403      BEQ     MTRYB         ;BRANCH IF GOOD
8097                                ;ERROR! R6 IMPROPERLY DECREMENTED
8098                                ;OR CPU ERROR REGISTER NOT CORRECT
8099 031672 1#:
8100 031672 104000      ERROR                                ;ALL ERRORS TO TRAP TO EMT VECTOR
8101 031674 001002      .WORD 1002                                ;UNIQUE ERROR NUMBER
8102 031676 001127      .WORD CPUERR                                ;ADDRESS OF ERROR MESSAGE
8103 031700 MTRYB:
8104 031700 005067 146062      CLR      CPEREG        ;CLEAR THE CPU ERROR REGISTER
8105 031704 016767 147120 146072      MOV      SLOC00,4     ;RESTORE VECTOR
8106 031712 010167 146230      MOV      R1,146      ;RESTORE VECTORS
8107 031716 010267 146222      MOV      R2,144      ;
8108 031722 010367 146214      MOV      R3,142      ;
8109 031726 012706 001000      MOV      #STBOT,R6  ;
8110
8111
8112
8113 031732      ;
8114 MTRYM:
8115      ;*****
8116      ;*TEST 220      TEST STACK OVERFLOW TRAPS IN VARIOUS MODES
8117      ;*****
8118      ;TST220:
8119      ;
8120      ;
8121      ;
8122      ;
8123      ;
8124      ;
8125      ;
8126      ;
8127      ;
8128      ;
8129      ;
8130      ;
8131      ;
8132      ;
8133      ;
8134      ;
8135      ;
8136      ;
8137      ;
8138      ;
8139      ;
8140      ;
8141      ;
8142      ;

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8143 032044 012706 000150          MOV      #150,R6          ; SETUP OVERFLOW R6 DATA
8144 032050 012767 032072 145726    MOV      #TRYMC,4
8145 032056 044546                    BIC      -(R5),-(R6)      ; CAUSE OVERFLOW TRAP
8146 032060 012706 001000          MOV      #STBOT,R6      ; RESTORE R6 FOR ERROR CALL
8147                                ; NO OVERFLOW TRAP
8148 032064 104000                    ERROR
8149 032066 001005                    .WORD   1005             ; ALL ERRORS TO TRAP TO EMT VECTOR
8150 032070 001127                    .WORD   CPUERR          ; UNIQUE ERROR NUMBER
8151 032072 005067 145670          TRYMC:  CLR      CPEREG   ; ADDRESS OF ERROR MESSAGE
8152 032076 016767 146726 145700    MOV      SLOC00,4       ; CLEAR CPU ERROR REGISTER
8153 032104 012706 001000          MOV      #STBOT,R6     ; RESTORE VECTOR
8154
8155
8156
8157 032110          ;
8158                                ; MILLO:
8159                                ; *****
8160                                ; *TEST 221      TEST STACK OVERFLOW ON ILLEGAL INST TRAP
8161                                ; *****
8161 032110          TST221:
8162 032110 005267 146670          INC      #TESTN         ; INCREMENT TEST NUMBER
8163 032114 005067 145646          CLR      CPEREG        ; CLEAR CPU ERROR REGISTER
8164 032120 012706 000400          MOV      #400,R6       ; SETUP FOR OVERFLOW TRAP
8165 032124 016767 145660 146676    MOV      10,SLOC00     ; SAVE VECTOR
8166 032132 012767 032160 145650    MOV      #MILLOA,10    ; SETUP ILLEGAL TRAP VECTOR
8167 032140 016767 145640 146664    MOV      4,SLOC01      ; SAVE VECTOR
8168 032146 012767 032172 145630    MOV      #MILLOB,4     ; SETUP OVERFLOW TRAP VECTOR
8169 032154 000077                    77                    ; UNUSED INSTRUCTION TRAP
8170 032156 000240                    NOP
8171 032160 012706 001000          MILLOA: MOV      #STBOT,R6 ; RESTORE R6 FOR ERROR CALL
8172                                ; UNUSED INSTRUCTION TRAP
8173 032164 104000                    ERROR
8174 032166 001006                    .WORD   1006           ; ALL ERRORS TO TRAP TO EMT VECTOR
8175 032170 001127                    .WORD   CPUERR        ; UNIQUE ERROR NUMBER
8176 032172                                ; ADDRESS OF ERROR MESSAGE
8177 032172 016767 146634 145604    MOV      SLOC01,4      ; RESTORE VECTOR
8178 032200 016767 146624 145602    MOV      SLOC00,10     ; RESTORE VECTOR
8179 032206 005067 145554          CLR      CPEREG        ; CLEAR CPU ERROR REGISTER
8180 032212 012706 001000          MOV      #STBOT,R6     ; RESTORE R6
8181
8182
8183
8184
8185 032216          ;
8186                                ; MIOTO:
8187                                ; *****
8188                                ; *TEST 222      TEST STACK OVERFLOW ON IOT TRAP
8189                                ; *****
8189 032216 005267 146562          TST222:
8190 032216 005067 145540          INC      #TESTN         ; INCREMENT TEST NUMBER
8191 032222 005067 145540          CLR      CPEREG        ; CLEAR CPU ERROR REGISTER
8192 032226 012706 000400          MOV      #400,R6       ; SETUP STACK FOR OVERFLOW
8193 032232 016767 145562 146570    MOV      20,SLOC00     ; SAVE OLD IOT VECTOR
8194 032240 012767 032266 145552    MOV      #IOTOA,20     ; SETUP ERROR ACTION ON IOT
8195 032246 016767 145532 146556    MOV      4,SLOC01      ; SAVE VECTOR
8196 032254 012767 032300 145522    MOV      #IOTOB,4      ; SETUP CORRECT TRAP VECTOR FOR
8197                                ; OVERFLOW
8198 032262 000004          IOT                    ; TEST INSTRUCTION

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8199 032264 000240      NOP
8200 032266 012706 001000      IOTOA: MOV      #STBOT,R6          ;RESTORE R6 FOR ERROR CALL
8201                                     ;FAILURE OF STACK OVERFLOW
8202 032272 104000      ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
8203 032274 001007      .WORD 1007                               ;UNIQUE ERROR NUMBER
8204 032276 001127      .WORD CPUERR                             ;ADDRESS OF ERROR MESSAGE
8205 032300      IOTOB:
8206 032300 005067 145462      CLR      CPEREG                          ;CLEAR CPU ERROR REGISTER
8207 032304 012706 001000      MOV      #STBOT,R6
8208 032310 016767 146516 145466      MOV      SLOC01,4                       ;RESTORE VECTOR
8209 032316 016767 146506 145474      MOV      SLOC00,20                      ;RESTORE TRAP VECTOR
8210
8211 ;
8212 ;
8213 032324      ;MEMTO:
8214 ;*****
8215 ;*TEST 223      TEST STACK OVERFLOW ON EMT TRAP
8216 ;*****
8217 032324      TST223:
8218 032324 005267 146454      INC      #TESTN                          ;INCREMENT TEST NUMBER
8219 032330 005067 145432      CLR      CPEREG                          ;CLEAR CPU ERROR REGISTER
8220 032334 012706 000400      MOV      #400,R6                         ;SETUP STACK FOR OVERFLOW
8221 032340 016767 145464 146462      MOV      30,SLOC00                       ;SAVE OLD EMT VECTOR
8222 032346 012767 032374 145454      MOV      #EMTOA,30                       ;SETUP ERROR ACTION ON EMT
8223 032354 016767 145424 146450      MOV      4,SLOC01                        ;SAVE VECTOR
8224 032362 012767 032406 145414      MOV      #EMTOB,4                         ;SETUP CORRECT TRAP VECTOR FOR
8225                                     ;OVERFLOW
8226 032370 104000      EMT
8227 032372 000240      NOP
8228 032374 012706 001000      EMTOA: MOV      #STBOT,R6          ;RESTORE R6 FOR ERROR CALL
8229                                     ;FAILURE OF STACK OVERFLOW
8230 032400 104000      ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
8231 032402 001010      .WORD 1010                               ;UNIQUE ERROR NUMBER
8232 032404 001127      .WORD CPUERR                             ;ADDRESS OF ERROR MESSAGE
8233 032406      EMTOB:
8234 032406 016767 146416 145414      MOV      SLOC00,30                       ;RESTORE TRAP VECTOR
8235 032414 016767 146412 145362      MOV      SLOC01,4                       ;RESTORE VECTOR
8236 032422 005067 145340      CLR      CPEREG                          ;CLEAR CPU ERROR REGISTER
8237 032426 012706 001000      MOV      #STBOT,R6
8238
8239 032432      MTRPO:
8240 ;*****
8241 ;*TEST 224      TEST STACK OVERFLOW ON TRAP
8242 ;*****
8243 032432      TST224:
8244 032432 005267 146346      INC      #TESTN                          ;INCREMENT TEST NUMBER
8245 032436 005067 145324      CLR      CPEREG                          ;CLEAR CPU ERROR REGISTER
8246 032442 012706 000400      MOV      #400,R6                         ;SETUP STACK FOR OVERFLOW
8247 032446 016767 145362 146354      MOV      34,SLOC00                       ;SAVE OLD TRP VECTOR
8248 032454 012767 032502 145352      MOV      #TRPOA,34                       ;SETUP ERROR ACTION ON TRP
8249 032462 016767 145316 146342      MOV      4,SLOC01                        ;SAVE VECTOR
8250 032470 012767 032520 145306      MOV      #TRPOB,4                         ;SETUP CORRECT TRAP VECTOR FOR
8251                                     ;OVERFLOW
8252 032476 104400      TRAP
8253 032500 000240      NOP
8254 032502 010637 001062      TRPOA: MOV      SP,#SAVSP1          ;SAVE ERROR DATA

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8255 032506 012706 001000      MOV      #STBOT,R6                ;RESTORE R6 FOR ERROR CALL
8256                                     ;FAILURE OF STACK OVERFLOW
8257 032512 104000      ERROR                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
8258 032514 001011      .WORD   1011                               ;UNIQUE ERROR NUMBER
8259 032516 001127      .WORD   CPUERR                             ;ADDRESS OF ERROR MESSAGE
8260 032520
8261 032520 016767 146304 145306 TRPOB:  MOV      SLOC00,34                ;RESTORE TRAP VECTOR
8262 032526 016767 146300 145250      MOV      SLOC01,4                ;RESTORE VECTOR
8263 032534 005067 145226      CLR      CPEREG                  ;CLEAR CPU ERROR REGISTER
8264 032540 012706 001000      MOV      #STBOT,R6
8265
8266
8267
8268 032544      ;
8269      ;
8270      ;MBPTO:
8271      ;*****
8272      ;*TEST 225      TEST STACK OVERFLOW ON BPT
8273      ;*****
8274      ;TST225:
8275      ;INC      #TESTN                ;INCREMENT TEST NUMBER
8276      ;CLR      CPEREG                ;CLEAR CPU ERROR REGISTER
8277      ;MOV      #400,R6                ;SETUP STACK FOR OVERFLOW
8278      ;MOV      14,SLOC00              ;SAVE OLD BPT VECTOR
8279      ;MOV      #BPTOA,14             ;SETUP ERROR ACTION ON BPT
8280      ;MOV      4,SLOC01              ;SAVE VECTOR
8281      ;MOV      #BPTOB,4             ;SETUP CORRECT TRAP VECTOR FOR
8282      ;BPT                                     ;OVERFLOW
8283      ;NOP                                     ; TEST INSTRUCTION
8284      ;MOV      SP,#SAVSP1            ;SAVE ERROR DATA
8285      ;MOV      #STBOT,R6            ;RESTORE R6 FOR ERROR CALL
8286      ;ERROR                                     ;FAILURE OF STACK OVERFLOW
8287      ;.WORD   1012                               ;ALL ERRORS TO TRAP TO EMT VECTOR
8288      ;.WORD   CPUERR                             ;UNIQUE ERROR NUMBER
8289      ;BPTOB:                                     ;ADDRESS OF ERROR MESSAGE
8290      ;CLR      CPEREG                  ;CLEAR CPU ERROR REGISTER
8291      ;MOV      SLOC00,14              ;RESTORE TRAP VECTOR
8292      ;MOV      SLOC01,4              ;RESTORE VECTOR
8293      ;MOV      #STBOT,R6
8294
8295
8296
8297 032656      ;
8298      ;
8299      ;MILAO:
8300      ;*****
8301      ;*TEST 226      TEST STACK OVERFLOW AND ILLEGAL JMP INSTRUCTION
8302      ;*****
8303      ;TST226:
8304      ;INC      #TESTN                ;INCREMENT TEST NUMBER
8305      ;CLR      CPEREG                ;CLEAR CPU ERROR REGISTER
8306      ;MOV      #400,R6                ;SETUP STACK FOR OVERFLOW
8307      ;MOV      10,SLOC00              ;SAVE OLD ILLEGAL INST. VECTOR
8308      ;MOV      #ILA0A,10             ;SETUP ERROR ACTION ILLEGAL OPCODE
8309      ;MOV      4,SLOC01              ;SAVE VECTOR
8310      ;MOV      #ILB0B,4             ;SETUP CORRECT TRAP VECTOR FOR
8311      ;CLR      R1                                     ;OVERFLOW

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8311 032724 000101          JMP      R1                ; TEST INSTRUCTION
8312 032726 000240          NOP
8313 032730 012706 001000  ILA0A:  MOV      #STBOT,R6    ;RESTORE R6 FOR ERROR CALL
8314                                     ;FAILURE OF STACK OVERFLOW
8315 032734 104000          ERROR
8316 032736 001013          .WORD   1013             ;ALL ERRORS TO TRAP TO EMT VECTOR
8317 032740 001127          .WORD   CPUERR          ;UNIQUE ERROR NUMBER
8318 032742                                     ;ADDRESS OF ERROR MESSAGE
8319 032742 016767 146064 145034  ILB0B:  MOV      SLOC01,4        ;RESTORE VECTOR
8320 032750 016767 146054 145032  MOV      SLOC00,10       ;RESTORE TRAP VECTOR
8321 032756 005067 145004          CLR      CPEREG         ;CLEAR CPU ERROR REGISTER
8322 032762 012706 001000          MOV      #STBOT,R6
8323
8324
8325 032766          ;
8326          ;*****
8327          ;*TEST 227      TEST STACK OVERFLOW ON ILLEGAL JSR INST
8328          ;*****
8329 032766          TST227:
8330 032766 005267 146012          INC      $TESTN          ;INCREMENT TEST NUMBER
8331 032772 012706 000400          MOV      #400,R6        ;SETUP STACK FOR OVERFLOW
8332 032776 016767 145006 146024  MOV      10,SLOC00       ;SAVE OLD VECTOR
8333 033004 012767 033034 144776  MOV      #ILLB0A,10     ;SETUP ERROR ACTION ON ILL. OPCODE
8334 033012 016767 144766 146012  MOV      4,SLOC01        ;SAVE VECTOR
8335 033020 012767 033046 144756  MOV      #ILLB0B,4      ;SETUP CORRECT TRAP VECTOR FOR OVERFLOW
8336 033026 005001          CLR      R1
8337 033030 004501          JSR      R5,R1          ;*** TEST INSTRUCTION***
8338 033032 000240          NOP
8339 033034 012706 001000  ILLB0A: MOV      #STBOT,R6    ;RESTORE R6 FOR ERROR CALL
8340                                     ;ERROR!! FAILURE OF STACK OVERFLOW
8341 033040 104000          ERROR
8342 033042 001014          .WORD   1014             ;ALL ERRORS TO TRAP TO EMT VECTOR
8343 033044 001127          .WORD   CPUERR          ;UNIQUE ERROR NUMBER
8344 033046 005037 177766 144730  ILLB0B: CLR      #CPEREG    ;ADDRESS OF ERROR MESSAGE
8345 033052 016767 145752 144730  MOV      SLOC00,10       ;CLEAR CPU ERROR REGISTER
8346 033060 016767 145746 144716  MOV      SLOC01,4        ;RESTORE TRAP VECTOR
8347 033066 012706 001000          MOV      #STBOT,R6     ;RESTORE VECTOR
8348
8349
8350          ;
8351 033072          ;
8352          ;*****
8353          ;*TEST 230      TEST FOR FALSE STACK OVERFLOW
8354          ;*****
8355 033072          TST230:
8356 033072 005267 145706          INC      $TESTN          ;INCREMENT TEST NUMBER
8357 033076 016767 144702 145724  MOV      4,SLOC00       ;SAVE VECTOR
8358 033104 012767 033152 144672  MOV      #MSTOE,4       ;ANTICIPATE OVERFLOW ERROR
8359 033112 012706 001002          MOV      #1002,R6      ;SETUP LEGAL R6
8360 033116 005746          TST     -(R6)           ;TRY TO CAUSE STACK OVERFLOW
8361 033120 012706 002002          MOV      #2002,R6     ;SETUP LEGAL R6
8362 033124 005746          TST     -(R6)           ;TRY TO CAUSE STACK OVERFLOW
8363 033126 012706 004002          MOV      #4002,R6     ;SETUP LEGAL R6
8364 033132 005746          TST     -(R6)           ;TRY TO CAUSE STACK OVERFLOW
8365 033134 012706 010002          MOV      #10002,R6    ;SETUP LEGAL R6
8366 033140 005746          TST     -(R6)           ;TRY TO CAUSE STACK OVERFLOW

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8423	033312	005267	145466		INC	%TESTN	INCREMENT TEST NUMBER
8424	033316	012706	001000		MOV	%STBOT,R6	SETUP STACK
8425	033322	016767	144466	145500	MOV	14,SLOC00	SAVE OLD T-BIT VECTOR
8426	033330	012746	000020		MOV	%20,-(R6)	PUSH T-BIT
8427	033334	012746	033356		MOV	%MTTSA,-(R6)	SETUP ERROR TRAP VECTOR
8428	033340	012767	033366	144446	MOV	%MTTSB,14	SETUP NEW T-BIT VECTOR
8429	033346	000006			RTT		CAUSE A T BIT SET IN PSW
8430							SHOULD NEVER BE EXECUTED
8431	033350	104000			ERROR		ALL ERRORS TO TRAP TO EMT VECTOR
8432	033352	001022			.WORD	1022	UNIQUE ERROR NUMBER
8433	033354	001127			.WORD	CPUERR	ADDRESS OF ERROR MESSAGE
8434	033356	000240			M.TSA: NOP		RTT WILL EXECUTE THIS INSTRUCTION
8435							WITH A T-BIT TRAP
8436							DIDNT TAKE CORRECT TRAP
8437	033360				MTTSQ:		
8438	033360	104000			ERROR		ALL ERRORS TO TRAP TO EMT VECTOR
8439	033362	001023			.WORD	1023	UNIQUE ERROR NUMBER
8440	033364	001127			.WORD	CPUERR	ADDRESS OF ERROR MESSAGE
8441	033366	022706	000774		MTTSB: CMP	%STBOT-4,R6	VERIFY SP DECIRMENT
8442	033372	001403			BEQ	MTTSD	BRANCH IF GOOD
8443							BAD SP
8444	033374	104000			ERROR		ALL ERRORS TO TRAP TO EMT VECTOR
8445	033376	001024			.WORD	1024	UNIQUE ERROR NUMBER
8446	033400	001127			.WORD	CPUERR	ADDRESS OF ERROR MESSAGE
8447	033402	021627	033360		MTTSD: CMP	(R6),%MTTSQ	VERIFY PC SAVED ON STACK
8448	033406	001403			BEQ	MTTSE	BRANCH IF GOOD
8449							INCORRECT PC ON STACK
8450	033410	104000			ERROR		ALL ERRORS TO TRAP TO EMT VECTOR
8451	033412	001025			.WORD	1025	UNIQUE ERROR NUMBER
8452	033414	001127			.WORD	CPUERR	ADDRESS OF ERROR MESSAGE
8453	033416				MTTSE:		
8454	033416	016767	145406	144370	MOV	SLOC00,14	RESTORE VECTOR 14
8455	033424	012706	001000		MOV	%STBOT,R6	
8456							
8457	033430				MTTR:		
8458							
8459							
8460							
8461	033430						
8462	033430	005267	145350				
8463	033434	012706	001000				
8464	033440	016767	144350	145362			
8465	033446	012746	000020				
8466	033452	012746	033504				
8467	033456	012767	033512	144330			
8468	033464	012767	000357	144304			
8469	033472	000277					
8470	033474	000002					
8471							
8472	033476	104000					
8473	033500	001026					
8474	033502	001127					
8475							
8476	033504						
8477	033504	104000					
8478	033506	001027					

8479	033510	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
8480	033512	026727	145260	000020	MTTRB:	CMP	STBOT-2,#20		: VERIFY PSW ON STACK
8481	033520	001403				BEQ	MTTRC		: BRANCH IF CORRECT STATUS
8482									: BAD STATUS ON STACK
8483	033522	104000				ERROR			: ALL ERRORS TO TRAP TO EMT VECTOR
8484	033524	001030				.WORD	1030		: UNIQUE ERROR NUMBER
8485	033526	001127				.WORD	CPUERR		: ADDRESS OF ERROR MESSAGE
8486	033530	012706	001000		MTTRC:	MOV	#STBOT,R6		: SETUP STACK
8487	033534	012746	000377			MOV	#377,-(R6)		: PUSH T-BIT
8488	033540	012746	033572			MOV	#MTTRD,-(R6)		: SETUP ERROR TRAP VECTOR
8489	033544	012767	033600	144242		MOV	#MTTRE,14		: SETUP NEW T-BIT VECTOR
8490	033552	012767	000000	144216		MOV	#0,PS		: CLEAR PRIORITY
8491	033560	000257				CCC			: CLEAR CONDITION CODES
8492	033562	000002				RTI			
8493									
8494	033564	104000				ERROR			: SHOULD NEVER EXECUTE
8495	033566	001031				.WORD	1031		: ALL ERRORS TO TRAP TO EMT VECTOR
8496	033570	001127				.WORD	CPUERR		: UNIQUE ERROR NUMBER
8497									: ADDRESS OF ERROR MESSAGE
8498	033572								: DIDNT TAKE CORRECT TRAP
8499	033572	104000			MTTRD:	ERROR			
8500	033574	001032				.WORD	1032		: ALL ERRORS TO TRAP TO EMT VECTOR
8501	033576	001127				.WORD	CPUERR		: UNIQUE ERROR NUMBER
8502	033600	026727	145172	000377	MTTRE:	CMP	STBOT-2,#377		: ADDRESS OF ERROR MESSAGE
8503	033606	001403				BEQ	MTTRF		: VERIFY OLD PSW ON STACK
8504									: BRANCH IF GOOD
8505	033610	104000				ERROR			: OLD PSW INCORRECT
8506	033612	001033				.WORD	1033		: ALL ERRORS TO TRAP TO EMT VECTOR
8507	033614	001127				.WORD	CPUERR		: UNIQUE ERROR NUMBER
8508	033616								: ADDRESS OF ERROR MESSAGE
8509	033616	016767	145206	144170	MTTRF:	MOV	SLOC00,14		
8510	033624	012706	001000			MOV	#STBOT,R6		: RESTORE VECTOR
8511									
8512									
8513	033630								
8514									
8515									
8516									
8517	033630								
8518	033630	005267	145150			INC	#TESTN		: INCREMENT TEST NUMBER
8519	033634	012706	001000			MOV	#STBOT,R6		: SETUP STACK
8520	033640	016767	144144	145162		MOV	10,SLOC00		: SAVE OLD VECTOR
8521	033646	012767	033664	144134		MOV	#MRTB,10		: SETUP NEW RESERVED VECTOR
8522	033654	000077				77			
8523									
8524	033656								: DIDNT TAKE CORRECT TRAP
8525	033656	104000			MRTA:	ERROR			
8526	033660	001034				.WORD	1034		: ALL ERRORS TO TRAP TO EMT VECTOR
8527	033662	001127				.WORD	CPUERR		: UNIQUE ERROR NUMBER
8528	033664	022706	000774		MRTB:	CMP	#STBOT-4,R6		: ADDRESS OF ERROR MESSAGE
8529	033670	001403				BEQ	MRTA		: VERIFY SP DECRIMENT
8530									: BRANCH IF GOOD
8531	033672	104000				ERROR			: BAD PC ON STACK
8532	033674	001035				.WORD	1035		: ALL ERRORS TO TRAP TO EMT VECTOR
8533	033676	001127				.WORD	CPUERR		: UNIQUE ERROR NUMBER
8534	033700	021627	033656		MRTA:	CMP	(R6),#MRTA		: ADDRESS OF ERROR MESSAGE
									: VERIFY PROPER PC ON STACK

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8535 033704 001403          BEQ      MRTF
8536                                ;BRANCH IF GOOD
8537 033706 104000          ERROR
8538 033710 001036          .WORD   1036
8539 033712 001127          .WORD   CPUERR
8540 033714                                ;ADDRESS OF ERROR MESSAGE
8541 033714 016767 145110 144066 MRTF:  MOV     SLOC00,10
8542 033722 012706 001000          MOV     #STBOT,R6
8543                                ;RESTORE TRAP VECTOR
8544
8545
8546 033726          ;
8547          ;
8548          ;MRT0:
8549          ;*****
8550          ;*TEST 235      TEST OLD STATUS ON RESERVED INST TRAP
8551          ;*****
8552          ;TST235:
8553          ;
8554          ;
8555          ;
8556          ;
8557          ;
8558          ;
8559          ;DIDNT TAKE CORRECT TRAP
8560 033762 104000          MRT0A:  ERROR
8561 033764 001037          .WORD   1037
8562 033766 001127          .WORD   CPUERR
8563 033770 026727 145002 000000 MRT0B:  CMP     STBOT-2,#0
8564 033776 001403          BEQ     MRT0C
8565                                ;BRANCH IF CORRECT STATUS
8566 034000 104000          ;BAD STATUS ON STACK
8567 034002 001040          ;ALL ERRORS TO TRAP TO EMT VECTOR
8568 034004 001127          ;UNIQUE ERROR NUMBER
8569 034006 012706 001000          ;ADDRESS OF ERROR MESSAGE
8570 034012 012767 034040 143770 MRT0C:  MOV     #STBOT,R6
8571 034020 012767 000357 143750          MOV     #MRT0E,10
8572 034026 000277          MOV     #357,PS
8573 034030 000077          SCC
8574                                77
8575                                ;RESERVED INSTRUCTION
8576 034032          ;DIDNT TAKE CORRECT TRAP
8577 034032 104000          MRT0D:  ERROR
8578 034034 001041          .WORD   1041
8579 034036 001127          .WORD   CPUERR
8580 034040 026727 144732 000357 MRT0E:  CMP     STBOT-2,#357
8581 034046 001403          BEQ     MRT0F
8582                                ;BRANCH IF GOOD
8583 034050 104000          ;OLD PSM INCORRECT
8584 034052 001042          ;ALL ERRORS TO TRAP TO EMT VECTOR
8585 034054 001127          ;UNIQUE ERROR NUMBER
8586 034056          ;ADDRESS OF ERROR MESSAGE
8587 034056 016767 144746 143724 MRT0F:  MOV     SLOC00,10
8588 034064 012706 001000          MOV     #STBOT,R6
8589                                ;RESOTRE TRAP VECTOR
8590 034070          MTP:

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8591
8592
8593
8594 034070
8595 034070 005267 144710
8596 034074 012706 001000
8597 034100 016767 143730 144722
8598 034106 012767 034132 143720
8599 034114 005067 143656
8600 034120 000257
8601 034122 104400
8602
8603 034124 MTPR:
8604 034124 104000
8605 034126 001043
8606 034130 001127
8607 034132 022706 000774 MTPB:
8608 034136 001403
8609
8610 034140 104000
8611 034142 001044
8612 034144 001127
8613 034146 021627 034124 MTPQ:
8614 034152 001403
8615
8616 034154 104000
8617 034156 001045
8618 034160 001127
8619 034162
8620 034162 016767 144642 143644 MTPF:
8621 034170 012706 001000
8622
8623
8624
8625 034174
8626
8627
8628
8629 034174
8630 034174 005267 144604
8631 034200 012706 001000
8632 034204 016767 143624 144616
8633 034212 012767 034236 143614
8634 034220 005067 143552
8635 034224 000257
8636 034226 104400
8637
8638 034230 MTPOA:
8639 034230 104000
8640 034232 001046
8641 034234 001127
8642 034236 026727 144534 000000 MTPOB:
8643 034244 001403
8644
8645 034246 104000
8646 034250 001047

;*****
; *TEST 236 TEST TRAP INST
;*****
TST236:
INC #TESTN ;INCREMENT TEST NUMBER
MOV #STBOT,R6 ;SETUP STACK
MOV 34,SLOC00 ;SAVE OLD VECTOR
MOV #MTPB,34 ;SETUP NEW TRAP VECTOR
CLR PS ;CLEAR PRIORITY ABND COND C
CCC
TRAP

;DIDNT TAKE CORRECT TRAP

MTPR:
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 1043 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
MTPB:
CMP #STBOT-4,R6 ;VERIFY SP DECRIMENT
BEQ MTPQ ;BRANCH IF GOOD
;BAD PC ON STACK

MTPQ:
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 1044 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
MTPF:
CMP (R6),#MTPR ;VERIFY PROPER PC ON STACK
BEQ MTPF ;BRANCH IF GOOD
;INCORRECT PC ON STACK

MTPF:
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 1045 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
MOV SLOC00,34 ;RESTORE VECTOR
MOV #STBOT,R6

;
;
MTPO:
;*****
; *TEST 237 TEST OLD STATUS SAVED ON TRAP
;*****
TST237:
INC #TESTN ;INCREMENT TEST NUMBER
MOV #STBOT,R6 ;SETUP STACK
MOV 34,SLOC00 ;SAVE OLD VECTOR
MOV #MTPOB,34 ;SETUP NEW TRAP VECTOR
CLR PS ;CLEAR PRIORITY AND COND C
CCC
TRAP

;DIDNT TAKE CORRECT TRAP

MTPOA:
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 1046 ;UNIQUE ERROR NUMBER
.WORD CPUERR ;ADDRESS OF ERROR MESSAGE
MTPOB:
CMP STBOT-2,#0 ;VERIFY PSW ON STACK
BEQ MTPOC ;BRANCH IF CORRECT STATUS
;BAD STATUS ON STACK

MTPOC:
ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
.WORD 1047 ;UNIQUE ERROR NUMBER

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8647 034252 001127
8648 034254 012706 001000
8649 034260 012767 034306 143546
8650 034266 012767 000357 143502
8651 034274 000277
8652 034276 104400
8653
8654 034300
8655 034300 104000
8656 034302 001050
8657 034304 001127
8658 034306 026727 144464 000357
8659 034314 001403
8660
8661 034316 104000
8662 034320 001051
8663 034322 001127
8664 034324
8665 034324 016767 144500 143502
8666 034332 012706 001000
8667
8668
8669
8670 034336
8671
8672
8673
8674 034336
8675 034336 005267 144442
8676 034342 005003
8677 034344 012706 001000
8678 034350 016767 143460 144452
8679 034356 016767 143422 144446
8680 034364 012767 034420 143412
8681 034372 012767 034426 143434
8682 034400 000167 000022
8683
8684 034404 000000
8685
8686 034406 104000
8687 034410 001052
8688 034412 001127
8689
8690
8691 034414 000167 000006
8692
8693
8694 034420
8695 034420 104000
8696 034422 001053
8697 034424 001127
8698
8699
8700 034426
8701 034426 005203
8702
    
```

```

; ADDRESS OF ERROR MESSAGE
; SETUP STACK
; SET UP TRAP VECTOR
; SET PRIORITY
; SET CONDITION CODES
; ISSUE TRAP
; DIDNT TAKE CORRECT TRAP

; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; VERIFY OLD PSW ON STACK
; BRANCH IF GOOD
; OLD PSW INCORRECT
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

; RESTORE TRAP VECTOR

;
;
; MTPA:
; *****
; *TEST 240 TEST ALL TRAP OPCODES - SELF MODIFYING
; *****
TST240:
    INC    #TESTN
    CLR    R3
    MOV    #STBOT,R6
    MOV    34,SLOC00
    MOV    4,SLOC01
    MOV    #MTPAH,4
    MOV    #MTPAA,34
    JMP    MTPAA
; INCREMENT TEST NUMBER
; SETUP REGISTER TO INDICATE OPCODE
; SETUP STACK
; SAVE OLD VECTOR
; SAVE IN CASE OF HALT
; SETUP HALT TRAP
; SETUP NEW TRAP VECTOR
; GO INTO LOOPING CODE

; MTPAL: HALT
; SET TO A ZERO
; TRAP INSTRUCTION FAILED TO TRAP
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; EXAMINE OPCCODE AT LOCATION MTPAL:

;
;
; MTPAH:
; ERROR
; .WORD 1052
; .WORD CPUERR
; ERROR, EITHER CANT MODIFY LOCATION MTPAL
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE

; OR TRAP INSTRUCTION FAILED
; GET NEXT OPCODE
    
```



```

8703 034430 012706 001000      MOV      #STBOT,R6      ;RESTORE STACK
8704 034434 020327 000400      CMP      R3,#400      ;SEE IF LAST OPCODE
8705 034440 001406              BEQ      MTPAE        ;BRANCH IF DONE
8706 034442 012767 104400 177734  MOV      #104400,MTPAL ;TRAP OPCODE INTO LOCATION
8707 034450 060367 177730      ADD      R3,MTPAL     ;FORM TEST OPCODE
8708 034454 000753              BR       MTPAL        ;EXECUTE TEST
8709 034456              MTPAE:
8710
8711 034456 016767 144346 143350      MOV      SLOC00,34
8712 034464 016767 144342 143312      MOV      SLOC01,4      ;RESTORE VECTORS
8713
8714 034472 012706 001000      MOV      #STBOT,R6
8715
8716
8717
8718 034476              ;
8719              ; MIOT:
8720              ;*****
8721              ;*TEST 241      TEST IOT TRAP
8722              ;*****
8723 034476 005267 144302      TST241:      INC      #TESTN      ;INCREMENT TEST NUMBER
8724 034502 012706 001000      MOV      #STBOT,R6      ;SETUP STACK
8725 034506 016767 143306 144314      MOV      20,SLOC00      ;SAVE OLD VECTOR
8726 034514 012767 034532 143276      MOV      #MIOTB,20      ;SETUP NEW IOT VECTOR
8727 034522 000004      IOT          ;***TEST INSTRUCTION***
8728              ;ERROR! DIDNT TAKE CORRECT TRAP
8729 034524      MIOTA:
8730 034524 104000      ERROR      ;ALL ERRORS TO TRAP TO EMT VECTOR
8731 034526 001054      .WORD     1054      ;UNIQUE ERROR NUMBER
8732 034530 001127      .WORD     CPUERR    ;ADDRESS OF ERROR MESSAGE
8733 034532 022706 000774      MIOTB:      CMP      #STBOT-4,R6  ;VERIFY SP DECRIMENT
8734 034536 001403      BEQ      MIOTD      ;BRANCH IF GOOD
8735              ;BAD PC ON STACK
8736 034540 104000      ERROR      ;ALL ERRORS TO TRAP TO EMT VECTOR
8737 034542 001055      .WORD     1055      ;UNIQUE ERROR NUMBER
8738 034544 001127      .WORD     CPUERR    ;ADDRESS OF ERROR MESSAGE
8739 034546 021627 034524      MIOTD:      CMP      (R6),#MIOTA  ;VERFY PROPER PC ON STACK
8740 034552 001403      BEQ      MIOTF      ;BRANCH IF GOOD
8741              ;INCORRECT PC ON STACK
8742 034554 104000      ERROR      ;ALL ERRORS TO TRAP TO EMT VECTOR
8743 034556 001056      .WORD     1056      ;UNIQUE ERROR NUMBER
8744 034560 001127      .WORD     CPUERR    ;ADDRESS OF ERROR MESSAGE
8745 034562 016767 144242 143230      MIOTF:      MOV      SLOC00,20      ;RESTORE VECTOR
8746 034570 012706 001000      MOV      #STBOT,R6
8747
8748 034574      MITO:
8749              ;*****
8750              ;*TEST 242      TEST OLD STATUS ON IOT TRAP
8751              ;*****
8752 034574 005267 144204      TST242:      INC      #TESTN      ;INCREMENT TEST NUMBER
8753 034600 012706 001000      MOV      #STBOT,R6      ;SETUP STACK
8754 034604 016767 143210 144216      MOV      20,SLOC00      ;SAVE OLD VECTOR
8755 034612 012767 034636 143200      MOV      #MITOB,20      ;SETUP NEW IOT VECTOR
8756 034620 005067 143152      CLR      PS          ;CLEAR PRIORITY AND COND C
8757 034624 000257      CCC

```

```

8759 034626 000004 IOT
8760
8761 034630 MITOA: ;DIDNT TAKE CORRECT TRAP
8762 034630 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
8763 034632 001057 .WORD 1057 ;UNIQUE ERROR NUMBER
8764 034634 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8765 034636 026727 144134 000000 MITOB: CMP STBOT-2,#0 ;VERIFY PSW ON STACK
8766 034644 001403 BEQ MITOC ;BRANCH IF CORRECT STATUS
8767
8768 034646 104000 ERROR ;BAD STATUS ON STACK
8769 034650 001060 .WORD 1060 ;ALL ERRORS TO TRAP TO EMT VECTOR
8770 034652 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
8771 034654 012706 001000 MITOC: MOV #STBOT,R6 ;ADDRESS OF ERROR MESSAGE
8772 034660 012767 034706 143132 MOV #MITOE,20 ;SETUP STACK
8773 034666 012767 000357 143102 MOV #357,PS ;SET UP TRAP VECTOR
8774 034674 000277 SCC ;SET PRIORITY
8775 034676 000004 IOT ;SET CONDITION CODES
8776
8777 034700 MITOD: ;DIDNT TAKE CORRECT TRAP
8778 034700 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
8779 034702 001061 .WORD 1061 ;UNIQUE ERROR NUMBER
8780 034704 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8781 034706 026727 144064 000357 MITOE: CMP STBOT-2,#357 ;VERIFY OLD PSW ON STACK
8782 034714 001403 BEQ MITOF ;BRANCH IF GOOD
8783
8784 034716 104000 ERROR ;OLD PSW INCORRECT
8785 034720 001062 .WORD 1062 ;ALL ERRORS TO TRAP TO EMT VECTOR
8786 034722 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
8787 034724 MITOF: ;ADDRESS OF ERROR MESSAGE
8788 034724 016767 144100 143066 MOV SLOC00,20 ;RESTORE VECTOR
8789 034732 012706 001000 MOV #STBOT,R6
8790
8791
8792 034736 ;
8793 ;MET:
8794 ;*****
8795 ;*TEST 243 TEST EMULATOR TRAP INSTRUCTION (EMT)
8796 ;*****
8796 034736 TST243:
8797 034736 005267 144042 INC #TESTN ;INCREMENT TEST NUMBER
8798 034742 012706 001000 MOV #STBOT,R6 ;SETUP STACK
8799 034746 016767 143056 144054 MOV 30,SLOC00 ;SAVE OLD VECTOR
8800 034754 012767 035006 143046 MOV #METB,30 ;SETUP NEW EMT VECTOR
8801 034762 016767 143046 144042 MOV 34,SLOC01 ;SAVE TRAP VECTOR
8802 034770 012767 043470 143036 MOV #ERROR,34 ;SET UP TO HANDLE EMT ERROR
8803 034776 104000 EMT
8804
8805 035000 META: ;DIDNT TAKE CORRECT TRAP
8806 035000 104400 TRAP ;ERROR TRAP
8807 035002 001063 .WORD 1063 ;ERROR NUMBER
8808 035004 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8809 035006 022706 000774 METB: CMP #STBOT-4,R6 ;VERIFY SP DECRIMENT
8810 035012 001403 BEQ METD ;BRANCH IF GOOD
8811
8812 035014 104000 ERROR ;BAD PC ON STACK
8813 035016 001064 .WORD 1064 ;ALL ERRORS TO TRAP TO EMT VECTOR
8814 035020 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
;ADDRESS OF ERROR MESSAGE

```


8815	035022	021627	035000			METD:	CMP	(R6),#META		:VERIFY PROPER PC ON STACK
8816	035026	001403					BEQ	METF		:BRANCH IF GOOD
8817										:INCORRECT PC ON STACK
8818	035030	104000					ERROR			:ALL ERRORS TO TRAP TO EMT VECTOR
8819	035032	001065					.WORD	1065		:UNIQUE ERROR NUMBER
8820	035034	001127					.WORD	CPUERR		:ADDRESS OF ERROR MESSAGE
8821	035036	016767	143770	142770		METF:	MOV	SLOC01,34		:RESTORE VECTOR
8822	035044	016767	143760	142756			MOV	SLOC00,30		:RESTORE VECTOR
8823	035052	012706	001000				MOV	#STBOT,R6		
8824										
8825										
8826	035056									
8827										
8828										
8829										
8830	035056									
8831	035056	005267	143722				INC	#TESTN		:INCREMENT TEST NUMBER
8832	035062	012706	001000				MOV	#STBOT,R6		:SETUP STACK
8833	035066	016767	142736	143734			MOV	30,SLOC00		:SAVE OLD VECTOR
8834	035074	012767	035134	142726			MOV	#METOB,30		:SETUP NEW EMT VECTOR
8835	035102	016767	142726	143722			MOV	34,SLOC01		:SAVE TRAP VECTOR
8836	035110	012767	043470	142716			MOV	#ERROR,34		:SET UP TRAP VECTOR
8837	035116	005067	142654				CLR	PS		:CLEAR PRIORITY AND COND C
8838	035122	000257					CCC			
8839	035124	104000					EMT			
8840										:DIDNT TAKE CORRECT TRAP
8841	035126									
8842	035126	104400				METOA:	TRAP			:ERROR TRAP
8843	035130	001066					.WORD	1066		:ERROR NUMBER
8844	035132	001127					.WORD	CPUERR		:ADDRESS OF ERROR MESSAGE
8845	035134	026727	143636	000000		METOB:	CMP	STBOT-2,#0		:VERIFY PSW ON STACK
8846	035142	001403					BEQ	METOC		:BRANCH IF CORRECT STATUS
8847										:BAD STATUS ON STACK
8848	035144	104000					ERROR			:ALL ERRORS TO TRAP TO EMT VECTOR
8849	035146	001067					.WORD	1067		:UNIQUE ERROR NUMBER
8850	035150	001127					.WORD	CPUERR		:ADDRESS OF ERROR MESSAGE
8851	035152	012706	001000			METOC:	MOV	#STBOT,R6		:SETUP STACK
8852	035156	012767	035204	142644			MOV	#METOE,30		:SET UP TRAP VECTOR
8853	035164	012767	000357	142604			MOV	#357,PS		:SET PRIORITY
8854	035172	000277					SCC			:SET CONDITION CODES
8855	035174	104000					EMT			
8856										:DIDNT TAKE CORRECT TRAP
8857	035176									
8858	035176	104400				METOD:	TRAP			:ERROR TRAP
8859	035200	001070					.WORD	1070		:ERROR NUMBER
8860	035202	001127					.WORD	CPUERR		:ADDRESS OF ERROR MESSAGE
8861	035204	026727	143566	000357		METOE:	CMP	STBOT-2,#357		:VERIFY OLD PSW ON STACK
8862	035212	001403					BEQ	METOF		:BRANCH IF GOOD
8863										:OLD PSW INCORRECT
8864	035214	104000					ERROR			:ALL ERRORS TO TRAP TO EMT VECTOR
8865	035216	001071					.WORD	1071		:UNIQUE ERROR NUMBER
8866	035220	001127					.WORD	CPUERR		:ADDRESS OF ERROR MESSAGE
8867	035222									
8868	035222	016767	143604	142604		METOF:	MOV	SLOC01,34		:RESTORE VECTOR
8869	035230	016767	143574	142572			MOV	SLOC00,30		:RESTORE VECTOR
8870	035236	012706	001000				MOV	#STBOT,R6		

```

8871
8872
8873
8874 035242
8875
8876
8877
8878 035242
8879 035242 005267 143536
8880 035246 012706 001000
8881 035252 016767 142536 143550
8882 035260 012767 035276 142526
8883 035266 000003
8884
8885 035270
8886 035270 104000
8887 035272 001072
8888 035274 001127
8889 035276 022706 000774
8890 035302 001403
8891
8892 035304 104000
8893 035306 001073
8894 035310 001127
8895 035312 021627 035270
8896 035316 001403
8897
8898 035320 104000
8899 035322 001074
8900 035324 001127
8901 035326 016767 143476 142460
8902 035334 012706 001000
8903
8904
8905
8906 035340
8907
8908
8909
8910 035340
8911 035340 005267 143440
8912 035344 012706 001000
8913 035350 016767 142440 143452
8914 035356 012767 035402 142430
8915 035364 005067 142406
8916 035370 000257
8917 035372 000003
8918
8919 035374
8920 035374 104000
8921 035376 001075
8922 035400 001127
8923 035402 026727 143370 000000
8924 035410 001403
8925
8926 035412 104000
    
```

```

;
;
; MBT:
;*****
; *TEST 245 TEST BPT TRAP
;*****
TST245:
    INC    #TESTN           ; INCREMENT TEST NUMBER
    MOV    #STBOT,R6       ; SETUP STACK
    MOV    14,SLOC00       ; SAVE OLD VECTOR
    MOV    #MBTB,14       ; SETUP NEW BPT VECTOR
    BPT
; DIDNT TAKE CORRECT TRAP
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; VERIFY SP DECRIEMENT
; BRANCH IF GOOD
; BAD PC ON STACK
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; VERIFY PROPER PC ON STACK
; BRANCH IF GOOD
; INCORRECT PC ON STACK
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; RESTORE VECTOR
    
```

```

;
;
; MBTA:
    ERROR .WORD 1072
    .WORD CPUERR
; MBTB:
    CMP    #STBOT-4,R6
    BEQ    MBTD
; MBTD:
    ERROR .WORD 1073
    .WORD CPUERR
    CMP    (R6),#MBTA
    BEQ    MBTF
; MBTF:
    ERROR .WORD 1074
    .WORD CPUERR
    MOV    SLOC00,14
    MOV    #STBOT,R6
    
```

```

;
;
; MBTO:
;*****
; *TEST 246 TEST OLD STATUS ON BPT TRAP
;*****
TST246:
    INC    #TESTN           ; INCREMENT TEST NUMBER
    MOV    #STBOT,R6       ; SETUP STACK
    MOV    14,SLOC00       ; SAVE OLD VECTOR
    MOV    #MBTOB,14      ; SETUP NEW BPT VECTOR
    CLR    PS              ; CLEAR PRIORITY AND COND C
    BPT
; DIDNT TAKE CORRECT TRAP
; ALL ERRORS TO TRAP TO EMT VECTOR
; UNIQUE ERROR NUMBER
; ADDRESS OF ERROR MESSAGE
; VERIFY PSW ON STACK
; BRANCH IF CORRECT STATUS
; BAD STATUS ON STACK
; ALL ERRORS TO TRAP TO EMT VECTOR
    
```

```

; MBTOA:
    ERROR .WORD 1075
    .WORD CPUERR
; MBTOB:
    CMP    STBOT-2,#0
    BEQ    MBTOC
; MBTOC:
    ERROR
    
```



```

8927 035414 001076 .WORD 1076 ;UNIQUE ERROR NUMBER
8928 035416 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8929 035420 012706 001000 MBTOC: MOV #STBOT,R6 ;SETUP STACK
8930 035424 012767 035452 142362 MOV #MBTOE,14 ;SET UP TRAP VECTOR
8931 035432 012767 000357 142336 MOV #357,PS ;SET PRIORITY
8932 035440 000277 SCC ;SET CONDITION CODES
8933 035442 000003 BPT
8934 ;
8935 035444 MBTOD: ;DIDNT TAKE CORRECT TRAP
8936 035444 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
8937 035446 001077 .WORD 1077 ;UNIQUE ERROR NUMBER
8938 035450 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8939 035452 026727 143320 000357 MBTOE: CMP STBOT-2,#357 ;VERIFY OLD PSW ON STACK
8940 035460 001403 BEQ MBTOF ;BRANCH IF GOOD
8941 ;
8942 035462 104000 ERROR ;OLD PSW INCORRECT
8943 035464 001100 .WORD 1100 ;ALL ERRORS TO TRAP TO EMT VECTOR
8944 035466 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
8945 035470 MBTOF: ;ADDRESS OF ERROR MESSAGE
8946 035470 016767 143334 142316 MOV SLOC00,14 ;RESTORE VECTOR
8947 035476 012706 001000 MOV #STBOT,R6
8948 ;
8949 ;
8950 ;
8951 035502 ;
8952 ;
8953 ;*****
8954 ;*TEST 247 TEST ILLEGAL JUMP INSTRUCTION TRAP
8955 ;*****
8956 035502 TST247: ;
8957 035502 005267 143276 INC #TESTN ;INCREMENT TEST NUMBER
8958 035506 012706 001000 MOV #STBOT,R6 ;SETUP STACK
8959 035512 016767 142272 143310 MOV 10,SLOC00 ;SAVE OLD VECTOR
8960 035520 012767 035540 142262 MOV #MILB,10 ;SETUP NEW ILLEGAL VECTOR
8961 035526 005001 CLR R1
8962 035530 000101 JMP R1 ;**TEST INSTRUCTIO
8963 ; ;DIDNT TAKE CORRECT TRAP
8964 035532 MILA: ;
8965 035532 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
8966 035534 001101 .WORD 1101 ;UNIQUE ERROR NUMBER
8967 035536 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8968 035540 022706 000774 MILB: CMP #STBOT-4,R6 ;VERIFY SP DECRIMENT
8969 035544 001403 BEQ MILD ;BRANCH IF GOOD
8970 ; ;BAD PC ON STACK
8971 035546 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
8972 035550 001102 .WORD 1102 ;UNIQUE ERROR NUMBER
8973 035552 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8974 035554 021627 035532 MILD: CMP (R6),#MILA ;VERFY PROPER PC ON STACK
8975 035560 001403 BEQ MILF ;BRANCH IF GOOD
8976 ; ;INCORRECT PC ON STACK
8977 035562 104000 ERROR ;ALL FRRORS TO TRAP TO EMT VECTOR
8978 035564 001103 .WORD 1103 ;UNIQUE ERROR NUMBER
8979 035566 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
8980 035570 016767 143234 142212 MILF: MOV SLOC00,10 ;RESTORE VECTOR
8981 035576 012706 001000 MOV #STBOT,R6
8982 035602 MILO:

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```

8983                                     ;*****
8984                                     ;*TEST 250      TEST OLD STATUS ON ILLEGAL JUMP TRAP
8985                                     ;*****
8986 035602                               TST250:
8987 035602 005267 143176                 INC    $TESTN           ;INCREMENT TEST NUMBER
8988 035606 012706 001000                 MOV    $STBOT,R6      ;SETUP STACK
8989 035612 016767 142172 143210         MOV    10,SLOC00     ;SAVE OLD VECTOR
8990 035620 012767 035646 142162         MOV    $MILOB,10     ;SETUP NEW ILLEGAL VECTOR
8991 035626 005067 142144                 CLR    PS             ;CLEAR PRIORITY AND COND C
8992 035632 000257                         CCC
8993 035634 005001                         CLR    R1
8994 035636 000101                         JMP    R1
8995                                     ;DIDNT TAKE CORRECT TRAP
8996 035640                               MILOA:
8997 035640 104000                         ERROR
8998 035642 001104                         .WORD
8999 035644 001127                         .WORD                ;ALL ERRORS TO TRAP TO EMT VECTOR
9000 035646 026727 143124 000004         MILOB: CMP    1104        ;UNIQUE ERROR NUMBER
9001 035654 001403                         BEQ    CPUERR         ;ADDRESS OF ERROR MESSAGE
9002                                     STBOT-2,#4
9003 035656 104000                         ERROR                ;BRANCH IF CORRECT STATUS
9004 035660 001105                         .WORD                ;BAD STATUS ON STACK
9005 035662 001127                         .WORD                ;ALL ERRORS TO TRAP TO EMT VECTOR
9006 035664 012706 001000                 MILOC: MOV    1105        ;UNIQUE ERROR NUMBER
9007 035670 012767 035716 142112         MOV    $STBOT,R6     ;ADDRESS OF ERROR MESSAGE
9008 035676 012767 000357 142072         MOV    $MILOE,10     ;SETUP STACK
9009 035704 000277                         MOV    $357,PS       ;SET UP TRAP VECTOR
9010 035706 000101                         SCC
9011                                     JMP    R1             ;SET PRIORITY
9012                                     ;SET CONDITION CODES
9013                                     ;DIDNT TAKE CORRECT TRAP
9014 035710                               MILOD:
9015 035710 104000                         ERROR
9016 035712 001106                         .WORD                ;ALL ERRORS TO TRAP TO EMT VECTOR
9017 035714 001127                         .WORD                ;UNIQUE ERROR NUMBER
9018 035716 026727 143054 000357         MILOE: CMP    1106        ;ADDRESS OF ERROR MESSAGE
9019 035724 001403                         BEQ    CPUERR         ;VERIFY OLD PSW ON STACK
9020                                     STBOT-2,#357
9021 035726 104000                         ERROR                ;BRANCH IF GOOD
9022 035730 001107                         .WORD                ;OLD PSW INCORRECT
9023 035732 001127                         .WORD                ;ALL ERRORS TO TRAP TO EMT VECTOR
9024 035734 016767 143070 142046         MILOF: MOV    1107        ;UNIQUE ERROR NUMBER
9025 035742 012706 001000                 MOV    SLOC00,10     ;ADDRESS OF ERROR MESSAGE
9026                                     MOV    $STBOT,R6     ;RESTORE VECTOR
9027                                     ;
9028 035746                               MIALL:
9029                                     ;*****
9030                                     ;*TEST 251      TEST ILLEGAL JSR INSTRUCTION TRAP
9031                                     ;*****
9032 035746                               TST251:
9033 035746 005267 143032                 INC    $TESTN           ;INCREMENT TEST NUMBER
9034 035752 012706 001000                 MOV    $STBOT,R6      ;SETUP STACK
9035 035756 016767 142026 143044         MOV    10,SLOC00     ;SAVE OLD VECTOR
9036 035764 012767 036004 142016         MOV    $MIALLB,10    ;SETUP NEW ILLEGAL VECTOR
9037 035772 005003                         CLR    R3
9038 035774 004303                         JSR   R3,R3

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9039                                     ;DIDNT TAKE CORRECT TRAP
9040 035776 MIALLA:                       ;ALL ERRORS TO TRAP TO EMT VECTOR
9041 035776 104000                       ;UNIQUE ERROR NUMBER
9042 036000 001110                       ;ADDRESS OF ERROR MESSAGE
9043 036002 001127                       ;VERIFY SP DECRIMENT
9044 036004 022706 000774 MIALLB: CMP    #STBOT-4,R6 ;BRANCH IF GOOD
9045 036010 001403 BEQ    MIALLD         ;BAD PC ON STACK
9046                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
9047 036012 104000                       ;UNIQUE ERROR NUMBER
9048 036014 001111                       ;ADDRESS OF ERROR MESSAGE
9049 036016 001127                       ;VERIFY PROPER PC ON STACK
9050 036020 021627 035776 MIALLD: CMP    (R6),#MIALLA ;BRANCH IF GOOD
9051 036024 001403 BEQ    MIALLF         ;INCORRECT PC ON STACK
9052                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
9053 036026 104000                       ;UNIQUE ERROR NUMBER
9054 036030 001112                       ;ADDRESS OF ERROR MESSAGE
9055 036032 001127                       ;VERIFY PROPER PC ON STACK
9056 036034 016767 142770 141746 MIALLF: MOV  SLOC00,10 ;RESTORE VECTOR
9057 036042 012706 001000 MOV    #STBOT,R6
9058
9059 ;
9060 ;
9061 036046 MJSI:
9062 ;*****
9063 ;*TEST 252 TEST OLD STATUS ON ILLEGAL JSR TRAP
9064 ;*****
9065 TST252:
9066 036046 005267 142732 INC    #TESTN           ;INCREMENT TEST NUMBER
9067 036052 012706 001000 MOV    #STBOT,R6       ;SETUP STACK
9068 036056 016767 141726 142744 MOV    10,SLOC00      ;SAVE OLD VECTOR
9069 036064 012767 036112 141716 MOV    #MJSIB,10     ;SETUP NEW VECTOR
9070 036072 005067 141700 CLR    PS           ;CLEAR PRIORITY AND COND C
9071 036076 000257 CCC
9072 036100 005003 CLR    R3
9073 036102 004303 JSR    R3,R3
9074
9075                                     ;DIDNT TAKE CORRECT TRAP
9076 036104 MJSIA:                       ;ALL ERRORS TO TRAP TO EMT VECTOR
9077 036106 104000                       ;UNIQUE ERROR NUMBER
9078 036110 001113                       ;ADDRESS OF ERROR MESSAGE
9079 036112 026727 142660 000004 MJSIB: CMP    STBOT-2,#4 ;VERIFY PSW ON STACK
9080 036120 001403 BEQ    MJSIC         ;BRANCH IF CORRECT STATUS
9081                                     ;BAD STATUS ON STACK
9082                                     ;ALL ERRORS TO TRAP TO EMT VECTOR
9083 036124 104000                       ;UNIQUE ERROR NUMBER
9084 036126 001127                       ;ADDRESS OF ERROR MESSAGE
9085 036130 012706 001000 MJSIC: MOV    #STBOT,R6       ;SETUP STACK
9086 036134 012767 036162 141646 MOV    #MJSIE,10     ;SET UP TRAP VECTOR
9087 036142 012767 000357 141626 MOV    #357,PS      ;SET PRIORITY
9088 036150 000277 SCC
9089 036152 004303 JSR    R3,R3         ;SET CONDITION CODES
9090
9091                                     ;DIDNT TAKE CORRECT TRAP
9092 036154 MJSID:                       ;ALL ERRORS TO TRAP TO EMT VECTOR
9093 036156 104000                       ;UNIQUE ERROR NUMBER
9094 036160 001127                       ;ADDRESS OF ERROR MESSAGE

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9095 036162 026727 142610 000357 MJSIE: CMP STBOT-2,#357 ;VERIFY OLD PSW ON STACK
9096 036170 001403 BEQ MJSIF ;BRANCH IF GOOD
9097 ; ;OLD PSW INCORRECT
9098 036172 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
9099 036174 001116 .WORD 1116 ;UNIQUE ERROR NUMBER
9100 036176 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
9101 036200 MJSIF:
9102 036200 016767 142624 141602 MOV SLOC00,10 ;RESTORE VECTOR
9103 036206 012706 001000 MOV #STBOT,R6
9104 ;
9105 ;
9106 ;
9107 ;*****
9108 ;*TEST 253 I/O TIME OUT TEST
9109 ;*****
9110 036212 TST253:
9111 036212 005267 142566 INC #TESTN ;INCREMENT TEST NUMBER
9112 036216 005067 141544 CLR CPREG ;CLEAR CPU ERROR REGISTER
9113 036222 016767 141556 142600 MOV 4,SLOC00 ;SAVE VECTOR
9114 036230 012767 036256 141546 MOV #2#,4 ;SET UP VECTOR TO HANDLE NXM
9115 036236 012767 030000 141532 MOV #30000,PS ;INIT THE PSW TO A KNOWN STATE
9116 036244 005737 177700 TST #177700 ;TRY TO ACCESS HARDWARE ADDRESS
9117 ; ;FOR GENERAL PURPOSE REG 0. THIS
9118 ; ;IS NOT IMPLEMENTED ON KDJ11
9119 ; ;SHOULD CAUSE TIME OUT.
9120 036250 1#:
9121 036250 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
9122 036252 001117 .WORD 1117 ;UNIQUE ERROR NUMBER
9123 036254 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
9124 036256 022767 000020 141502 2#: CMP #BIT04,CPREG ;IS CPU ERROR REGISTER CORRECT?
9125 036264 001403 BEQ 3#
9126 036266 104000 ERROR ;ALL ERRORS TO TRAP TO EMT VECTOR
9127 036270 001120 .WORD 1120 ;UNIQUE ERROR NUMBER
9128 036272 001127 .WORD CPUERR ;ADDRESS OF ERROR MESSAGE
9129 036274 022627 036250 3#: CMP (SP),#1# ;CHECK THAT STACK CONTAINS CORRECT ADDR.
9130 036300 001403 BEQ 4#
9131 036302 104000 ERROR ;
9132 036304 001121 .WORD 1121 ;ALL ERRORS TO TRAP TO EMT VECTOR
9133 036306 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
9134 036310 022627 030000 4#: CMP (SP),#30000 ;ADDRESS OF ERROR MESSAGE
9135 036314 001403 BEQ 5# ;IS THE PSW OK?
9136 036316 104000 ERROR ;
9137 036320 001122 .WORD 1122 ;ALL ERRORS TO TRAP TO EMT VECTOR
9138 036322 001127 .WORD CPUERR ;UNIQUE ERROR NUMBER
9139 036324 005067 141436 5#: CLR CPREG ;ADDRESS OF ERROR MESSAGE
9140 036330 016767 142474 141446 MOV SLOC00,4 ;CLEAR THE CPU ERROR REGISTER
9141 ; ;RESTORE VECTOR
9142 ; ;*****
9143 ;*TEST 254 ODD ADDRESS/ILLEGAL INST FETCH TRAP TEST
9144 ; ;*****
9145 ;THIS PROGRAM GENERATES AN ODD ADDRESS IN THE PC. THE KDJ11 SHOULD
9146 ;TRAP THROUGH ADDR 4
9147 ; ;*****
9148 036336 TST254:
9149 036336 005267 142442 INC #TESTN ;INCREMENT TEST NUMBER
9150 036342 005067 141420 CLR CPREG ;INIT THE CPU ERROR REG

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SW4	= 000020	284#			
SW5	= 000040	283#			
SW6	= 000100	282#			
SW7	= 000200	281#			
SW8	= 000400	280#			
SW9	= 001000	279#			
SXT	= ***** U	5126			
SXTCC	= ***** U	5038			
S11	= ***** U	2706			
S22	= ***** U	2852			
S33	= ***** U	2974			
S77	= ***** U	3118			
TAGRAM	= 000001	1#	738		
TA114	021552	5897	5905#		
TA116	023620	6425	6434	6469#	6493
TBITVE	= 000014	321#			
TB114	021566	5906	5912#		
TC114	021602	5913	5919#		
TD114	021616	5920	5926#		
TE102	017756	5376#			
TE103	020010	5393#			
TE104	020042	5410#			
TE105	020074	5427#			
TE106	020126	5444#			
TE107	020160	5461#			
TE110	020212	5478#			
TE111	020244	5495#			
TE112	020276	5512#			
TE113	020574	5611#			
TE113A	021070	5710#			
TE114	021356	5852#			
TE115	023060	6293#			
TE115A	023330	6301	6324	6347	6381#
TE115B	023340	6302	6325	6348	6385#
TE115C	023346	6303	6326	6388#	
TE115D	023354	6349	6391#		
TE115F	023362	6377	6394#		
TE116	023364	6396#			
TE116A	023674	6421	6430	6496#	
TE116B	023700	6405	6431	6500#	
TE116C	023712	6414	6422	6505#	
TE116D	023722	6404	6413	6423	6432
TE117	023732	6516#			6509#
TE117A	024070	6523	6562#		
TE120	024076	6570#			
TE120A	024162	6580	6594#		
TE121	024262	6626#			
TE122	024730	6752#			
TE123	025214	6838#			
TE124	025470	6926#			
TE125	025756	7018#			
TE125A	026266	7025	7069	7123#	
TE126	026514	7214#			
TE126A	026572	7225	7234#		
TE126B	027366	7368	7421#		
TE127	027704	7543#			

TE127A	030154	7592	7635#						
TE130	030414	7737#							
TE130A	030762	7811	7862#						
TF114	021632	5927	5933#						
TG114	021646	5934	5940#						
TH114	021662	5941	5947#						
TKVEC	= 000060	328#							
TP	= ***** U	8590							
TPA	= ***** U	8670							
TPO	= ***** U	8625							
TPVEC	= 000064	329#	9599	9600	9601*	9602*	9625*	9626*	
TRAPVE	= 000034	327#	702*	703*					
TRPO	= ***** U	8239							
TRPOA	032502	8248	8254#						
TRPOB	032520	8250	8260#						
TRTVEC	= 000014	322#							
TRY	= ***** U	8071							
TRYM	= ***** U	8113							
TRYMA	032002	8122	8130#						
TRYMB	032040	8134	8141#						
TRYMC	032072	8144	8151#						
TSGPRO	= ***** U	875							
TSGPR1	= ***** U	912							
TSGPR2	= ***** U	949							
TSGPR3	= ***** U	986							
TSGPR4	= ***** U	1023							
TSGPR5	= ***** U	1060							
TSGPR6	= ***** U	1097							
TSMUO	014130	4116#							
TSPSWB	= ***** U	1134							
TSTLOC	001076	644#							
TST1	001510	753#							
TST10	002044	916#							
TST100	010072	2978#							
TST101	010172	3012#							
TST102	010272	3053#							
TST103	010362	3093#							
TST104	010446	3122#							
TST105	010550	3155#							
TST106	010636	3189#							
TST107	010732	3226#							
TST11	002146	953#							
TST110	011024	3263#							
TST111	011114	3297#							
TST112	011164	3323#							
TST113	011236	3349#							
TST114	011304	3373#							
TST115	011356	3397#							
TST116	011422	3419#							
TST117	011454	3439#							
TST12	002250	990#							
TST120	011512	3462#							
TST121	012070	3588#							
TST122	012434	3708#							
TST123	012624	3781#							
TST124	013476	3987#							

TST125	014030	4079#
TST126	014130	4120#
TST127	014746	4315#
TST13	002352	1027#
TST130	015026	4350#
TST131	015112	4387#
TST132	015200	4425#
TST133	015262	4461#
TST134	015360	4506#
TST135	015454	4552#
TST136	015550	4596#
TST137	015652	4643#
TST14	002454	1064#
TST140	016020	4713#
TST141	016104	4749#
TST142	016204	4793#
TST143	016310	4845#
TST144	016412	4899#
TST145	016516	4936#
TST146	016622	4988#
TST147	016736	5042#
TST15	002556	1101#
TST150	017022	5080#
TST151	017134	5134#
TST152	017276	5195#
TST153	017372	5232#
TST154	017466	5270#
TST155	017672	5346#
TST156	017724	5363#
TST157	017756	5380#
TST16	002664	1138#
TST160	020010	5397#
TST161	020042	5414#
TST162	020074	5431#
TST163	020126	5448#
TST164	020160	5465#
TST165	020212	5482#
TST166	020244	5499#
TST167	020276	5516#
TST17	003006	1177#
TST170	020574	5615#
TST171	021070	5714#
TST172	021356	5856#
TST173	021664	5953#
TST174	022236	6075#
TST175	022340	6112#
TST176	022442	6149#
TST177	022544	6186#
TST2	001550	785#
TST20	003044	1202#
TST200	022646	6223#
TST201	022750	6260#
TST202	023060	6297#
TST203	023364	6400#
TST204	023732	6520#
TST205	024076	6574#

TST206	024262	6630#
TST207	024730	6756#
TST21	003104	1229#
TST210	025214	6842#
TST211	025470	6930#
TST212	025756	7022#
TST213	026514	7218#
TST214	027704	7547#
TST215	030414	7741#
TST216	031372	8020#
TST217	031570	8075#
TST22	003150	1258#
TST220	031732	8117#
TST221	032110	8161#
TST222	032216	8189#
TST223	032324	8217#
TST224	032432	8243#
TST225	032544	8272#
TST226	032656	8301#
TST227	032766	8329#
TST23	003222	1290#
TST230	033072	8355#
TST231	033176	8384#
TST232	033312	8422#
TST233	033430	8461#
TST234	033630	8517#
TST235	033726	8550#
TST236	034070	8594#
TST237	034174	8629#
TST24	003300	1323#
TST240	034336	8674#
TST241	034476	8722#
TST242	034574	8752#
TST243	034736	8796#
TST244	035056	8830#
TST245	035242	8878#
TST246	035340	8910#
TST247	035502	8955#
TST25	003356	1356#
TST250	035602	8986#
TST251	035746	9032#
TST252	036046	9065#
TST253	036212	9110#
TST254	036336	9148#
TST255	036626	9224#
TST256	037046	9278#
TST257	037114	9298#
TST26	003430	1387#
TST260	037250	9351#
TST261	037354	9390#
TST262	037464	9431#
TST263	037552	9467#
TST264	040002	9550#
TST265	040134	9592#
TST266	040314	9639#
TST267	040374	9665#

TST27	003510	1421#	
TST270	040556	9714#	
TST271	040712	9748#	
TST272	040750	9768#	
TST273	041046	9802#	
TST274	041144	9830#	
TST275	041416	9891#	
TST276	041550	9929#	
TST3	001600	807#	
TST30	003564	1453#	
TST31	003730	1517#	
TST32	004012	1552#	
TST33	004110	1596#	
TST34	004172	1631#	
TST35	004326	1694#	
TST36	004444	1741#	
TST37	004602	1799#	
TST4	001630	827#	
TST40	004710	1842#	
TST41	004772	1873#	
TST42	005020	1896#	
TST43	005100	1931#	
TST44	005150	1962#	
TST45	005230	1997#	
TST46	005314	2034#	
TST47	005376	2070#	
TST5	001660	846#	
TST50	005462	2107#	
TST51	005562	2150#	
TST52	005646	2187#	
TST53	005734	2225#	
TST54	006006	2257#	
TST55	006062	2289#	
TST56	006130	2319#	
TST57	006206	2353#	
TST6	001710	862#	
TST60	006270	2387#	
TST61	006360	2425#	
TST62	006414	2447#	
TST63	006460	2476#	
TST64	006530	2507#	
TST65	006610	2541#	
TST66	006710	2583#	
TST67	007022	2632#	
TST7	001742	879#	
TST70	007152	2686#	
TST71	007220	2710#	
TST72	007270	2734#	
TST73	007374	2779#	
TST74	007474	2820#	
TST75	007562	2856#	
TST76	007646	2888#	
TST77	007754	2929#	
TT	= ***** U	8380	8418
TTR	= ***** U	8457	
TYPDS	= 104405	9992	10328#

TYPE	104401	9980	9990	9993	10060	10182	10251	10324#	10405	10408	10411
TYP0C =	104402	10325#	10410	10413							
TYP0N =	104404	10327#									
TYP0S =	104403	10326#									
T114	021524	5871	5884	5896#							
T116	023556	6407	6416	6449#	6466						
T122A	025042	6762	6776	6789#							
T122B	025174	6760	6828#								
T123A	025426	6847	6905#								
T123B	025436	6909#									
T123C	025444	6912#									
T123D	025452	6851	6916#								
T123E	025460	6895	6921#								
T123F	025464	6902	6923#								
T124A	025714	6935	6998#								
T124B	025724	7002#									
T124C	025732	7005#									
T124D	025740	6939	7009#								
T124E	025746	6988	7013#								
T124F	025752	6995	7015#								
UDPAR0=	177660	379#									
UDPAR1=	177662	380#									
UDPAR2=	177664	381#									
UDPAR3=	177666	382#									
UDPAR4=	177670	383#									
UDPAR5=	177672	384#									
UDPAR6=	177674	385#									
UDPAR7=	177676	386#									
UDPDR0=	177620	357#									
UDPDR1=	177622	358#									
UDPDR2=	177624	359#									
UDPDR3=	177626	360#									
UDPDR4=	177630	361#									
UDPDR5=	177632	362#									
UDPDR6=	177634	363#									
UDPDR7=	177636	364#									
UIPAR0=	177640	368#									
UIPAR1=	177642	369#									
UIPAR2=	177644	370#									
UIPAR3=	177646	371#									
UIPAR4=	177650	372#									
UIPAR5=	177652	373#									
UIPAR6=	177654	374#									
UIPAR7=	177656	375#									
UIPDR0=	177600	346#									
UIPDR1=	177602	347#									
UIPDR2=	177604	348#									
UIPDR3=	177606	349#									
UIPDR4=	177610	350#									
UIPDR5=	177612	351#									
UIPDR6=	177614	352#									
UIPDR7=	177616	353#									
UNXPIR	037346	9302	9376#								
WAITIN	001074	641#	9726	9776	9809	9837	9848	9859	9872	9897	
XBUF =	177566	499#									
XCSR =	177564	498#	9603*	9611*							

		7019#	7215#	7544#	7738#	8017#	8072#	8114#	8158#	8186#	8214#	8240#	8269#	8298#
		8326#	8352#	8381#	8419#	8458#	8514#	8547#	8591#	8626#	8671#	8719#	8749#	8793#
		8827#	8875#	8907#	8952#	8983#	9029#	9062#	9107#	9142#	9144	9221#	9275#	9295#
		9344#	9346	9385#	9387	9425#	9427	9456#	9458	9538#	9540	9589#	9633#	9635
		9659#	9661	9708#	9710	9742#	9744	9762#	9764	9791#	9793	9827#	9888#	9926#
\$OCNT	043146	10223#	10252#	10265#										
\$OMODE	043150	10218#	10222#	10227	10230#	10241#	10267#							
\$PASS	001006	589#	704#	730#	9596	9978	9982#	9983#	9991	10004				
\$PASTM	000212	565#												
\$PATCH	043636 G	10422#												
\$QUES	042474	10121#												
\$RDCHR=	***** U	10331												
\$RDDEC=	***** U	10331												
\$RDLIN=	***** U	10331												
\$RDOCT=	***** U	10331												
\$RTNAD	042030	10003#												
\$R2A =	***** U	10331												
\$SAVRE=	***** U	10331												
\$SETUP=	000126	508#	699	700	702	704	706	707	9982					
\$STUP =	177777	508#												
\$SVPC =	000204	540#	545											
\$SWR =	160000	212	213#	707	755	787	809	829	848	864	881	918	955	992
		1029	1066	1103	1140	1179	1204	1231	1260	1292	1325	1358	1389	1423
		1455	1519	1554	1598	1633	1696	1743	1801	1844	1878	1898	1933	1964
		1999	2036	2072	2109	2152	2189	2227	2259	2291	2321	2355	2389	2427
		2449	2478	2509	2543	2585	2634	2688	2712	2736	2781	2822	2858	2890
		2931	2980	3014	3055	3095	3124	3157	3191	3228	3265	3299	3325	3351
		3375	3399	3421	3441	3464	3590	3710	3783	3989	4081	4122	4317	4352
		4389	4427	4463	4508	4554	4598	4645	4715	4751	4795	4847	4901	4938
		4990	5044	5082	5136	5197	5234	5272	5348	5365	5382	5399	5416	5433
		5450	5467	5484	5501	5518	5617	5716	5858	5955	6077	6114	6151	6188
		6225	6262	6299	6402	6522	6576	6632	6758	6844	6932	7024	7220	7549
		7743	8022	8077	8119	8163	8191	8219	8245	8274	8303	8331	8357	8386
		8424	8463	8519	8552	8596	8631	8676	8724	8754	8798	8832	8880	8912
		8957	8988	9034	9067	9112	9150	9226	9280	9300	9353	9392	9433	9469
		9552	9594	9641	9667	9716	9750	9770	9804	9832	9893	9931	9974	9982
		9996	10002	10004										
\$SWREG	001022	597#	733											
\$TESTN	001004	588#	738#	754#	786#	808#	828#	847#	863#	880#	917#	954#	991#	1028#
		1065#	1102#	1139#	1178#	1203#	1230#	1259#	1291#	1324#	1357#	1388#	1422#	1454#
		1518#	1553#	1597#	1632#	1695#	1742#	1800#	1843#	1877#	1897#	1932#	1963#	1998#
		2035#	2071#	2108#	2151#	2188#	2226#	2258#	2290#	2320#	2354#	2388#	2426#	2448#
		2477#	2508#	2542#	2584#	2633#	2687#	2711#	2735#	2780#	2821#	2857#	2889#	2930#
		2979#	3013#	3054#	3094#	3123#	3156#	3190#	3227#	3264#	3298#	3324#	3350#	3374#
		3398#	3420#	3440#	3463#	3589#	3709#	3782#	3988#	4080#	4121#	4316#	4351#	4388#
		4426#	4462#	4507#	4553#	4597#	4644#	4714#	4750#	4794#	4846#	4900#	4937#	4989#
		5043#	5081#	5135#	5196#	5233#	5271#	5347#	5364#	5381#	5398#	5415#	5432#	5449#
		5466#	5483#	5500#	5517#	5616#	5715#	5857#	5954#	6076#	6113#	6150#	6187#	6224#
		6261#	6298#	6401#	6521#	6575#	6631#	6757#	6843#	6931#	7023#	7219#	7548#	7742#
		8021#	8076#	8118#	8162#	8190#	8218#	8244#	8273#	8302#	8330#	8356#	8385#	8423#
		8462#	8518#	8551#	8595#	8630#	8675#	8723#	8753#	8797#	8831#	8879#	8911#	8956#
		8987#	9033#	9066#	9111#	9149#	9225#	9279#	9299#	9352#	9391#	9432#	9468#	9551#
		9593#	9640#	9666#	9715#	9718#	9749#	9769#	9803#	9831#	9892#	9930#		
\$TKB	042462	10086	10093	10114#										
\$TKS	042460	10084	10091	10113#										
\$TN =	000277	212#	748	755#	780	787#	804	809#	824	829#	843	848#	859	864#

	876	881#	913	918#	950	955#	987	992#	1024	1029#	1061	1066#	1098	
	1103#	1135	1140#	1172	1179#	1199	1204#	1226	1231#	1255	1260#	1287	1292#	
	1320	1325#	1353	1358#	1384	1389#	1418	1423#	1450	1455#	1514	1519#	1549	
	1554#	1593	1598#	1628	1633#	1691	1696#	1738	1743#	1796	1801#	1839	1844#	
	1873	1878#	1893	1898#	1928	1933#	1959	1964#	1994	1999#	2031	2036#	2067	
	2072#	2104	2109#	2147	2152#	2184	2189#	2222	2227#	2254	2259#	2286	2291#	
	2316	2321#	2350	2355#	2384	2389#	2422	2427#	2444	2449#	2473	2478#	2504	
	2509#	2538	2543#	2580	2585#	2629	2634#	2683	2688#	2707	2712#	2731	2736#	
	2776	2781#	2817	2822#	2853	2858#	2885	2890#	2926	2931#	2975	2980#	3009	
	3014#	3050	3055#	3090	3095#	3119	3124#	3152	3157#	3186	3191#	3223	3228#	
	3260	3265#	3294	3299#	3320	3325#	3346	3351#	3370	3375#	3394	3399#	3416	
	3421#	3436	3441#	3459	3464#	3585	3590#	3705	3710#	3778	3783#	3984	3989#	
	4076	4081#	4117	4122#	4312	4317#	4347	4352#	4384	4389#	4422	4427#	4458	
	4463#	4501	4508#	4549	4554#	4593	4598#	4640	4645#	4710	4715#	4746	4751#	
	4790	4795#	4842	4847#	4893	4901#	4933	4938#	4985	4990#	5039	5044#	5077	
	5082#	5127	5136#	5192	5197#	5229	5234#	5267	5272#	5343	5348#	5360	5365#	
	5377	5382#	5394	5399#	5411	5416#	5428	5433#	5445	5450#	5462	5467#	5479	
	5484#	5496	5501#	5513	5518#	5612	5617#	5711	5716#	5853	5858#	5950	5955#	
	6072	6077#	6109	6114#	6146	6151#	6183	6188#	6220	6225#	6257	6262#	6294	
	6299#	6397	6402#	6517	6522#	6571	6576#	6627	6632#	6753	6758#	6839	6844#	
	6927	6932#	7019	7024#	7215	7220#	7544	7549#	7738	7743#	8017	8022#	8072	
	8077#	8114	8119#	8158	8163#	8186	8191#	8214	8219#	8240	8245#	8269	8274#	
	8298	8303#	8326	8331#	8352	8357#	8381	8386#	8419	8424#	8458	8463#	8514	
	8519#	8547	8552#	8591	8596#	8626	8631#	8671	8676#	8719	8724#	8749	8754#	
	8793	8798#	8827	8832#	8875	8880#	8907	8912#	8952	8957#	8983	8988#	9029	
	9034#	9062	9067#	9107	9112#	9142	9150#	9221	9226#	9275	9280#	9295	9300#	
	9344	9353#	9385	9392#	9425	9433#	9456	9469#	9538	9552#	9589	9594#	9633	
	9641#	9659	9667#	9708	9716#	9742	9750#	9762	9770#	9791	9804#	9827	9832#	
	9888	9893#	9926	9931#										
\$TPB	042466	10102#	10116#											
\$TPFLG	042473	10034	10120#											
\$TPS	042464	10100	10115#											
\$TRAP	043152	702	10276#											
\$TRAP2	043174	10287#	10323											
\$TRP =	000006	10316#	10325#	10326#	10327#	10328#	10329#							
\$TRPAD	043206	10281	10323#											
\$TSTM	000210	564#												
\$TSTNU=	000001	501#												
\$TYPBN=	***** U	10329												
\$TYPDS	042500	10136#	10328											
\$TYPE	042124	10034#	10316	10324	10362									
\$TYPEC	042336	10064	10071	10078	10083#									
\$TYPEX	042456	10106	10108	10111#										
\$TYPOC	042750	10221#	10325											
\$TYPON	042764	10220	10223#	10327										
\$TYPOS	042724	10216#	10326											
\$UNIT	001012	591#												
\$UNITM	000214	566#												
\$USWR	001024	598#												
\$XOFF =	000023	10088	10115											
\$XON =	000021	10095	10115											
\$\$GET4=	000000	9996#												
\$OFILL	043147	10217#	10221#	10231	10266#									
\$4OCAT	000000	526#												
.	= 043656	511#	527	531#	540	541#	543#	545#	551	552#	554#	556#	568#	
		573#	574#	645#	681#	10004	10005#	10016#	10113	10114	10115	10116	10117	10118

GLOBAL AREAS
KDJ11A.MAC

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0220

.\$ASTA= ***** U	10119	10120	10121	10122	10123#	10190#	10383#	10423#
.\$X = 000204	10335	10338						
	551#	556	568	573				

	5850	5892	6068	6105	6142	6179	6216	6253	6291	6378	6445	6558	6624	6749	6786
	6924	7016	7119	7417	7631	7858	8069	8110	8154	8183	8210	8238	8265	8294	8323
	8348	8377	8416	8456	8511	8543	8589	8622	8667	8715	8747	8790	8824	8871	8903
	8948	8981	9025	9058	9104	9141	9219	9272	9291	9339	9381	9420	9451	9533	9585
	9628	9656	9705	9740	9759	9789	9825	9886	9921	9965					
ERRDEF	1960	8805	8841	8857											
ERRDF	1970	764	773	790	797	817	835	851	868	885	892	899	906	922	929
	936	943	959	966	973	980	996	1003	1010	1017	1033	1040	1047	1054	1070
	1077	1084	1091	1107	1114	1121	1128	1144	1151	1158	1165	1183	1191	1209	1218
	1237	1247	1267	1279	1299	1312	1333	1345	1366	1376	1398	1410	1430	1442	1469
	1480	1494	1506	1529	1541	1566	1578	1585	1605	1620	1647	1658	1665	1676	1682
	1710	1721	1728	1758	1765	1772	1781	1788	1815	1822	1830	1853	1864	1884	1906
	1919	1942	1950	1973	1985	2010	2022	2048	2058	2083	2095	2122	2139	2167	2176
	2206	2214	2239	2246	2272	2279	2301	2308	2334	2342	2367	2376	2404	2413	2435
	2458	2465	2487	2496	2514	2522	2529	2554	2561	2569	2592	2601	2611	2621	2649
	2659	2675	2699	2722	2744	2751	2760	2768	2790	2800	2809	2836	2845	2868	2877
	2901	2911	2918	2941	2949	2958	2967	2992	2999	3022	3033	3042	3066	3074	3103
	3111	3135	3142	3165	3178	3200	3215	3236	3252	3275	3286	3312	3338	3362	3386
	3408	3428	3450	3470	3478	3490	3501	3509	3521	3529	3542	3550	3564	3577	3691
	3716	3730	3740	3756	3764	3795	3807	3823	3835	3850	3862	3879	3891	3907	3919
	3935	3947	3962	3974	4005	4025	4046	4065	4085	4093	4105	4111	4127	4135	4143
	4151	4161	4169	4177	4185	4200	4208	4216	4231	4239	4247	4260	4268	4276	4287
	4295	4303	4325	4338	4362	4375	4399	4413	4436	4449	4472	4492	4516	4529	4540
	4563	4574	4584	4606	4620	4631	4653	4666	4680	4692	4701	4724	4737	4762	4781
	4802	4812	4823	4833	4854	4864	4874	4884	4907	4912	4921	4926	4945	4955	4966
	4976	4997	5008	5018	5030	5053	5068	5091	5104	5117	5147	5163	5176	5185	5208
	5221	5247	5253	5260	5279	5287	5293	5300	5315	5323	5331	5337	5353	5370	5387
	5404	5421	5438	5455	5472	5489	5506	5524	5532	5541	5550	5559	5568	5577	5586
	5595	5604	5622	5631	5640	5649	5658	5667	5676	5685	5694	5703	5719	5725	5732
	5740	5748	5755	5764	5770	5777	5785	5794	5800	5807	5815	5824	5830	5837	5845
	5875	5888	5900	5908	5915	5922	5929	5936	5943	5965	5979	5985	5991	5997	6003
	6009	6015	6036	6042	6048	6054	6060	6065	6081	6088	6095	6102	6118	6125	6132
	6139	6155	6162	6169	6176	6192	6199	6206	6213	6229	6236	6243	6250	6266	6273
	6280	6287	6309	6316	6333	6340	6357	6364	6371	6442	6454	6461	6473	6480	6487
	6530	6536	6546	6553	6562	6586	6597	6604	6611	6617	6643	6651	6659	6668	6677
	6684	6691	6713	6723	6731	6739	6766	6780	6863	6870	6879	6887	6898	6916	6957
	6964	6973	6980	6991	7009	7036	7043	7050	7057	7081	7088	7096	7104	7111	7230
	7238	7248	7262	7269	7276	7287	7294	7301	7314	7322	7329	7336	7347	7354	7361
	7379	7386	7393	7400	7408	7556	7563	7574	7581	7588	7601	7608	7615	7623	7752
	7759	7766	7773	7785	7792	7799	7806	7821	7828	7835	7842	7850	8027	8036	8043
	8051	8058	8065	8089	8099	8127	8138	8148	8173	8202	8230	8257	8286	8315	8341
	8372	8393	8397	8404	8410	8431	8437	8444	8450	8472	8476	8483	8494	8498	8505
	8524	8531	8537	8559	8566	8576	8583	8603	8610	8616	8638	8645	8654	8661	8686
	8694	8729	8736	8742	8761	8768	8777	8784	8812	8818	8848	8864	8885	8892	8898
	8919	8926	8935	8942	8963	8970	8976	8996	9003	9012	9019	9040	9047	9053	9075
	9082	9091	9098	9120	9126	9131	9136	9159	9165	9170	9175	9190	9198	9203	9208
	9213	9240	9247	9253	9259	9264	9287	9314	9323	9363	9377	9400	9415	9448	9487
	9510	9520	9566	9574	9607	9615	9621	9652	9673	9687	9694	9699	9732	9756	9783
	9819	9842	9853	9866	9879	9901	9913	9937	9943	9958					
ERROR	2250	765	774	791	798	818	836	852	869	885	892	899	906	922	929
	936	943	959	966	973	980	996	1003	1010	1017	1033	1040	1047	1054	1070
	1077	1084	1091	1107	1114	1121	1128	1144	1151	1158	1165	1184	1192	1210	1219
	1238	1248	1268	1280	1299	1313	1333	1346	1366	1377	1398	1411	1430	1443	1469
	1481	1495	1507	1529	1542	1567	1579	1586	1605	1621	1648	1659	1666	1677	1683
	1711	1722	1729	1759	1766	1772	1782	1789	1816	1823	1831	1854	1865	1885	1907
	1920	1943	1951	1974	1986	2011	2023	2049	2059	2084	2096	2123	2140	2168	2177

